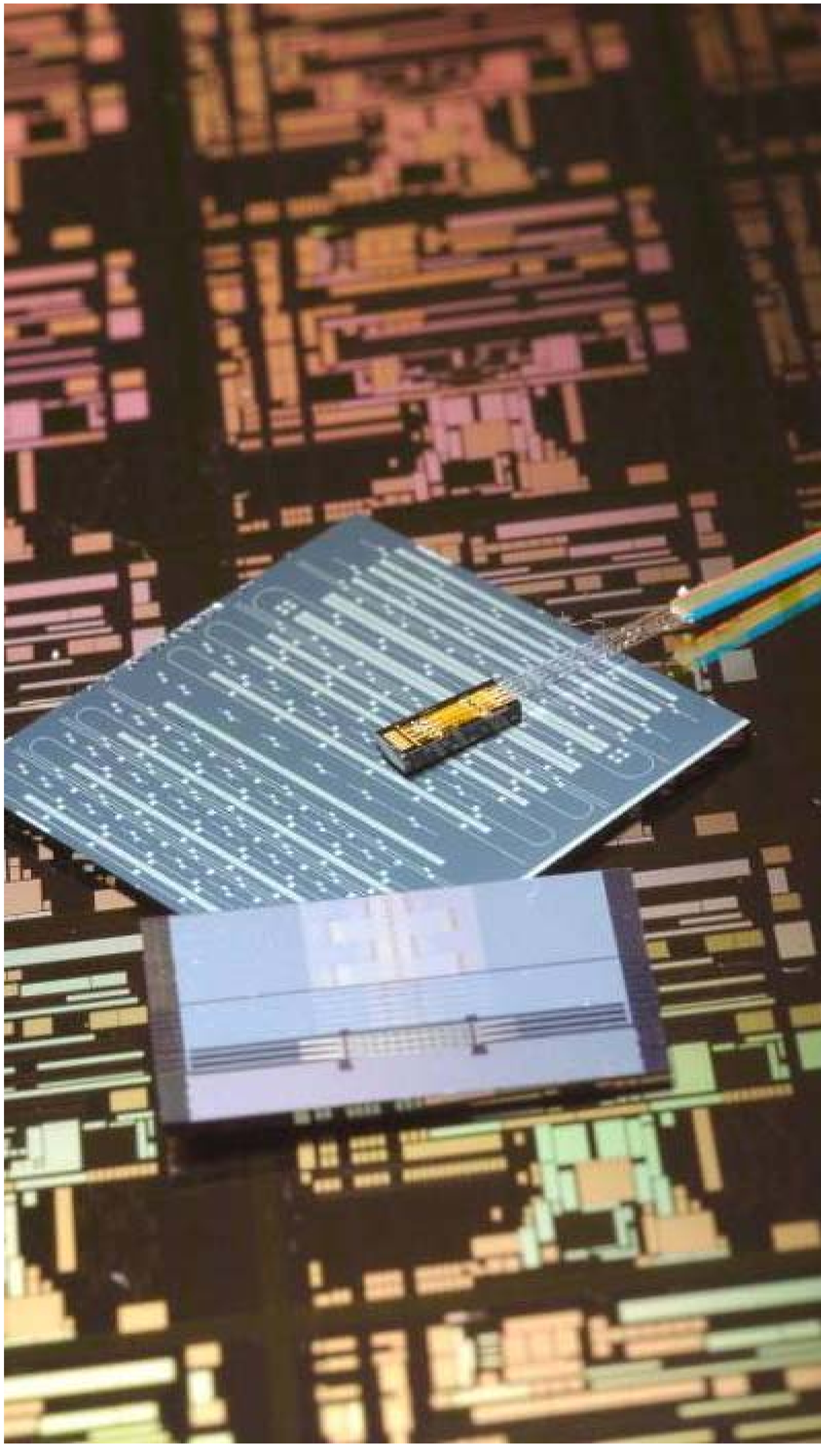


Silicon Photonics

Opportunity, applications & Recent Results

Dr. Mario Paniccia

Intel Fellow

Director, Photonics Technology Lab

Intel Corporation

www.intel.com/go/sp

Purdue University

Oct 5 2007

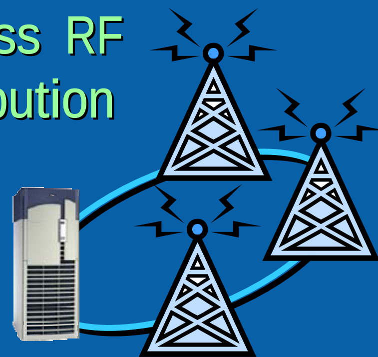
Agenda

- Motivation & applications
- History & progress
- Intel's Research Program
- Future work
- Summary

Photonics Applications

Enterprise Communication

Wireless RF Distribution



PC, Server Interconnects

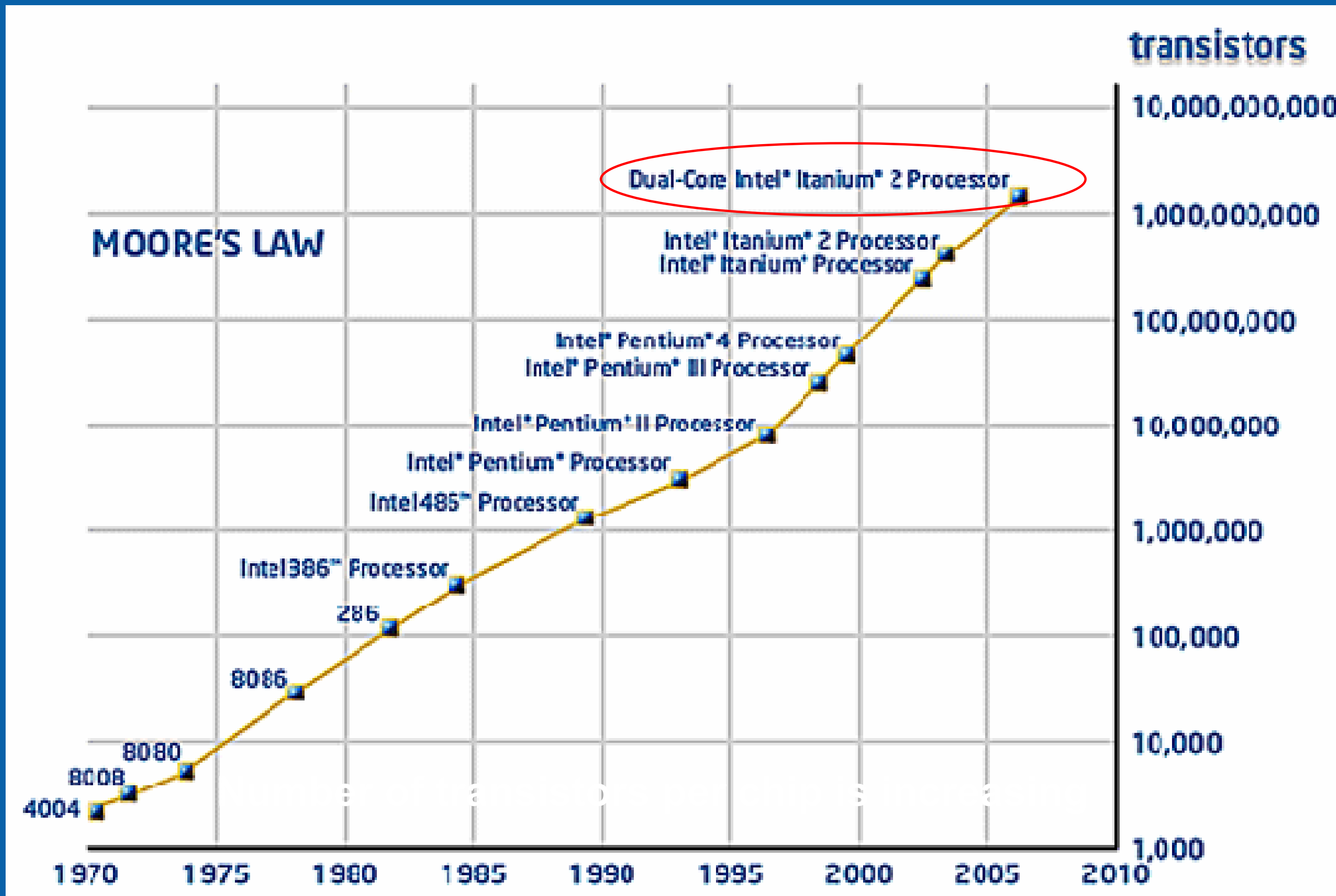
Health

Environmental Monitoring

Chemical Analysis

Photonics could impact all of these.
But today costs are prohibitive.

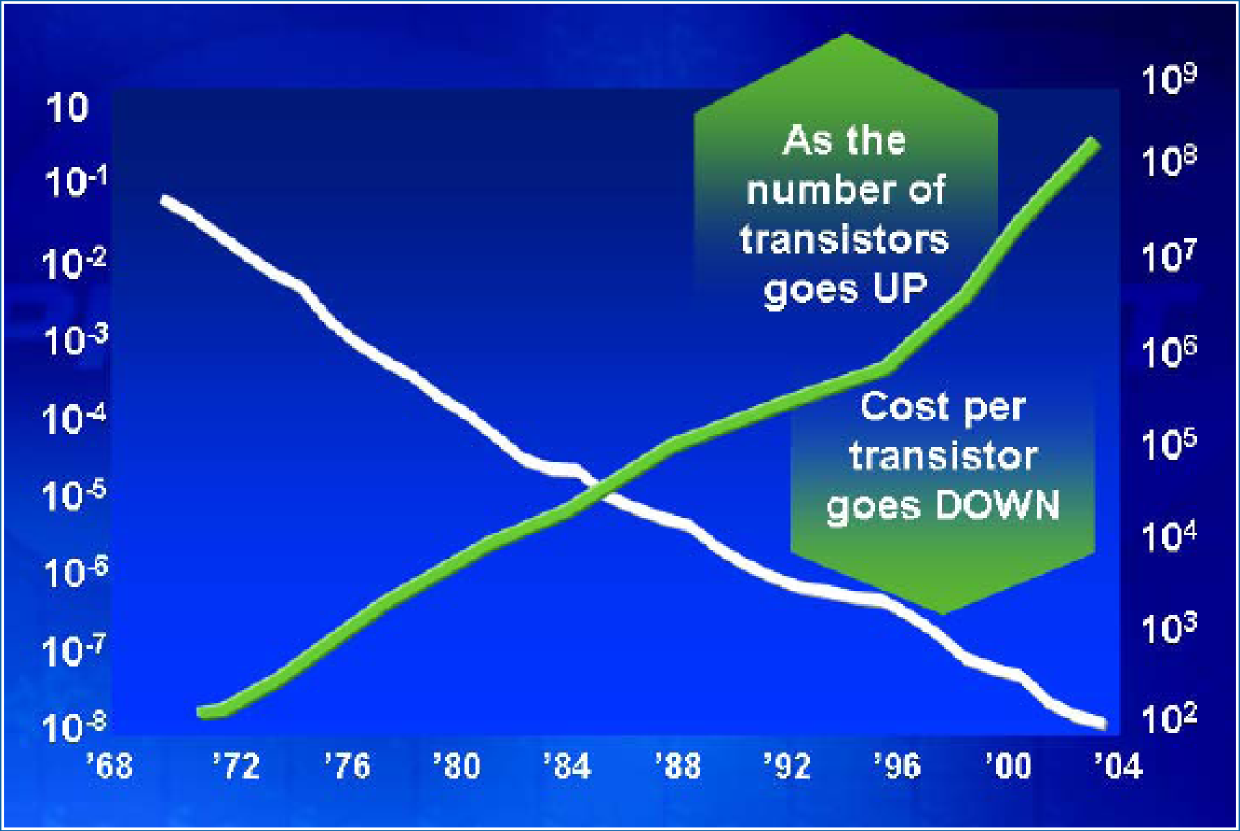
Processor History



Intel co-founder G. Moore predicted doubling of transistors approximately every 2 years (*Electronic Magazine, 1965)*

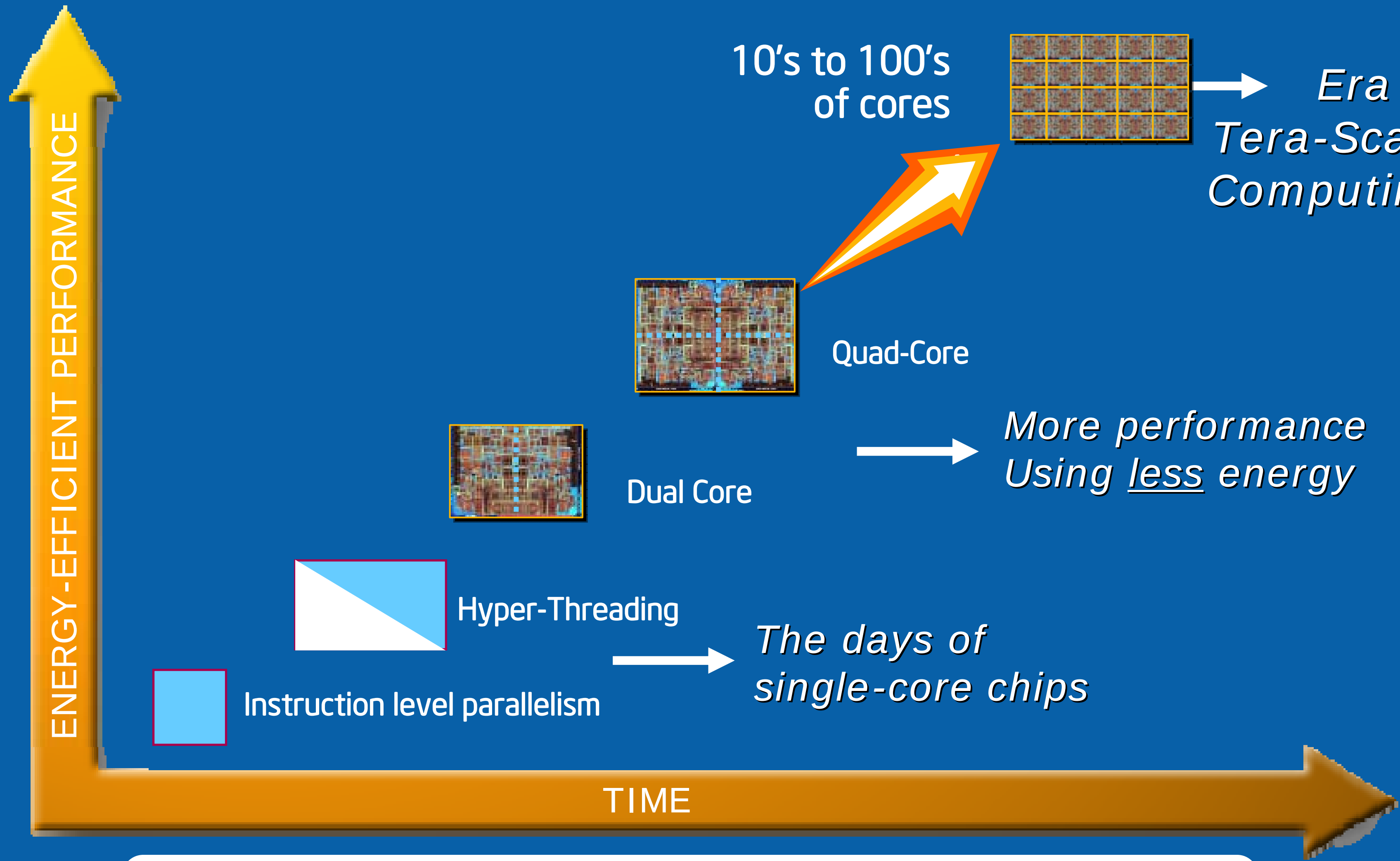
Electronics:
Economics of Moore's Law

SCALING + WAFER SIZE + HIGH VOLUME = LOWER COST



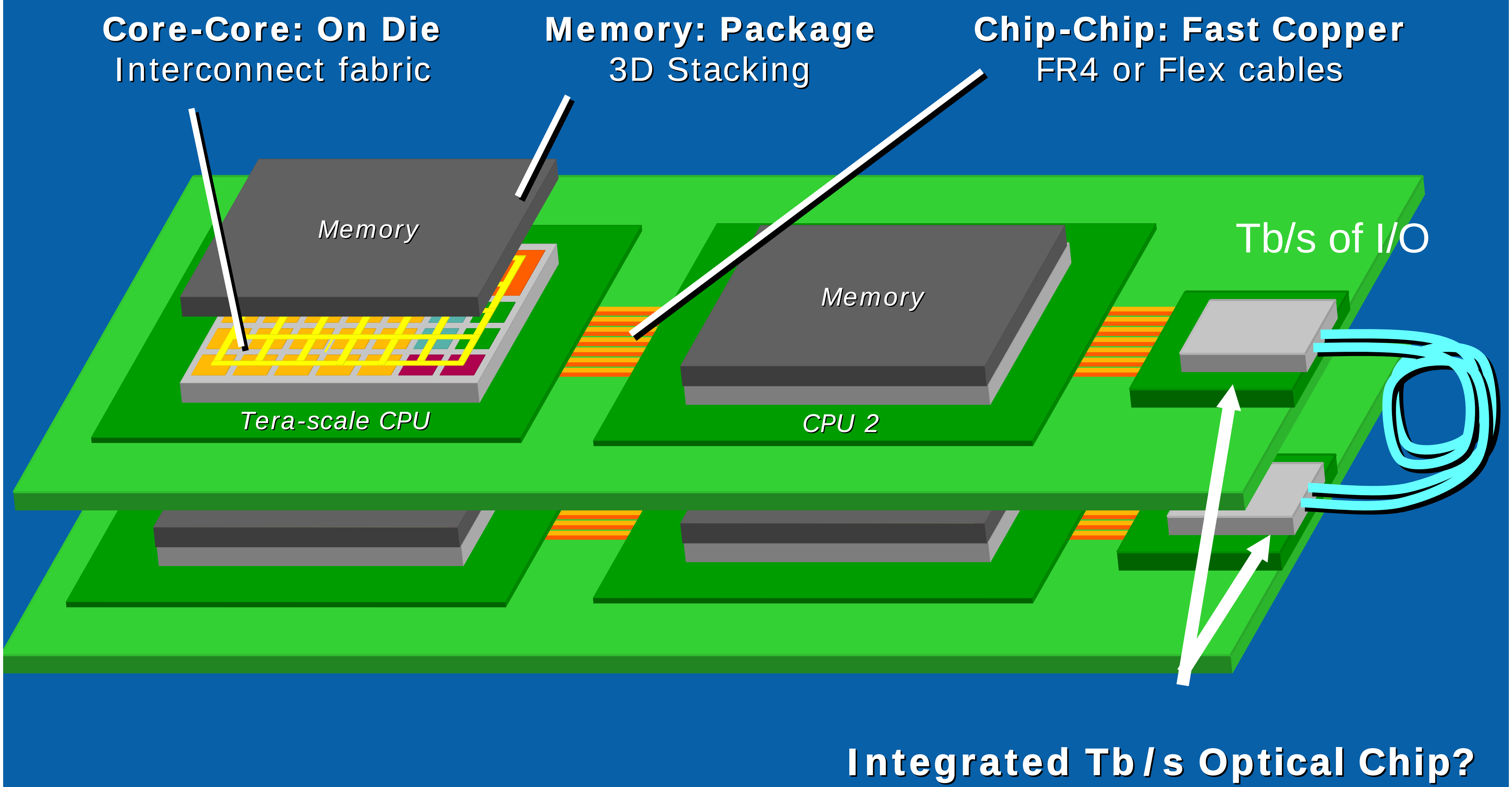
Integration & increased functionality

Tera-leap to Parallelism:

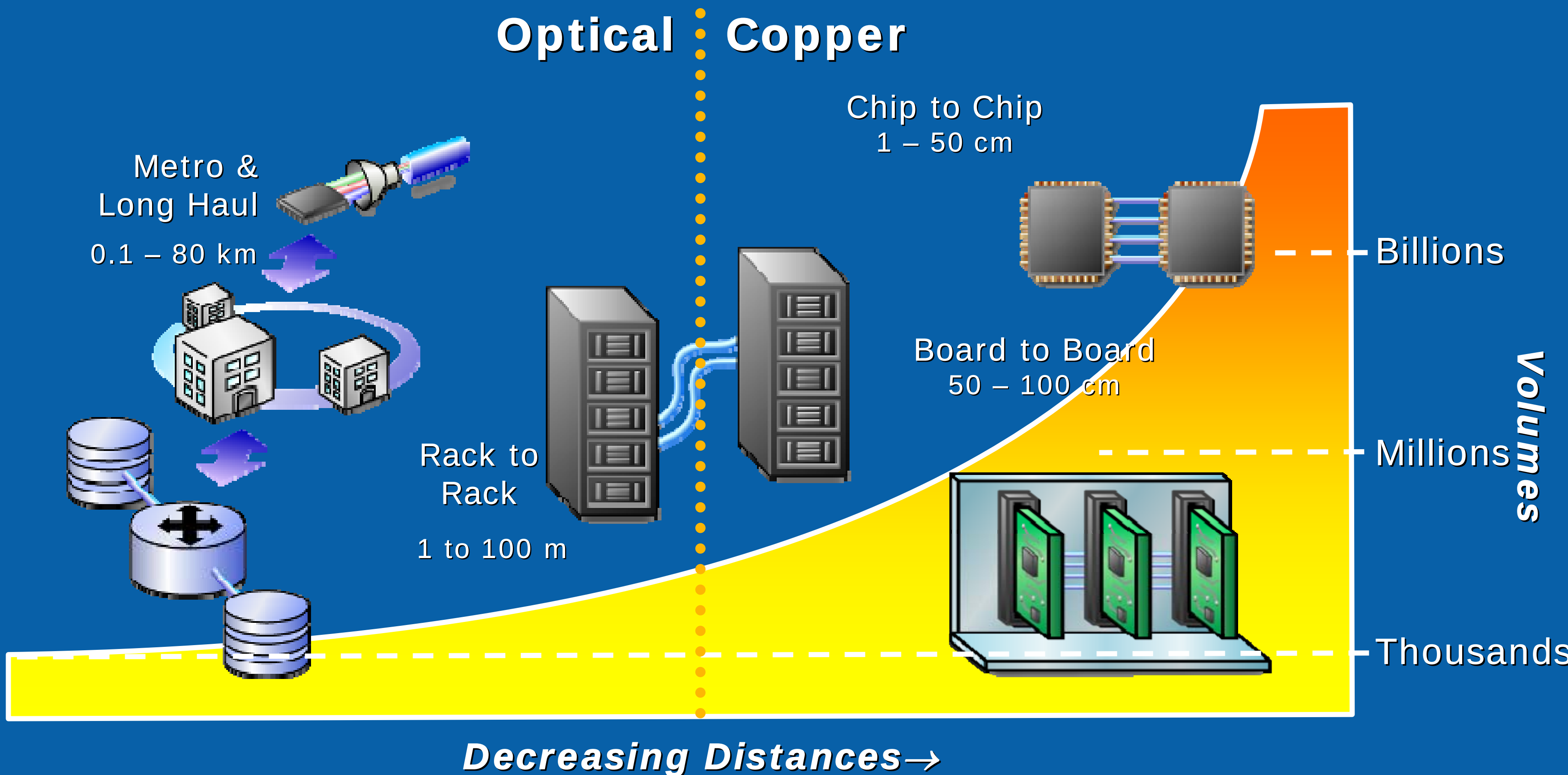


All this compute capability may require high speed optical links

Future Physical I/O for a Tera-scale Servers

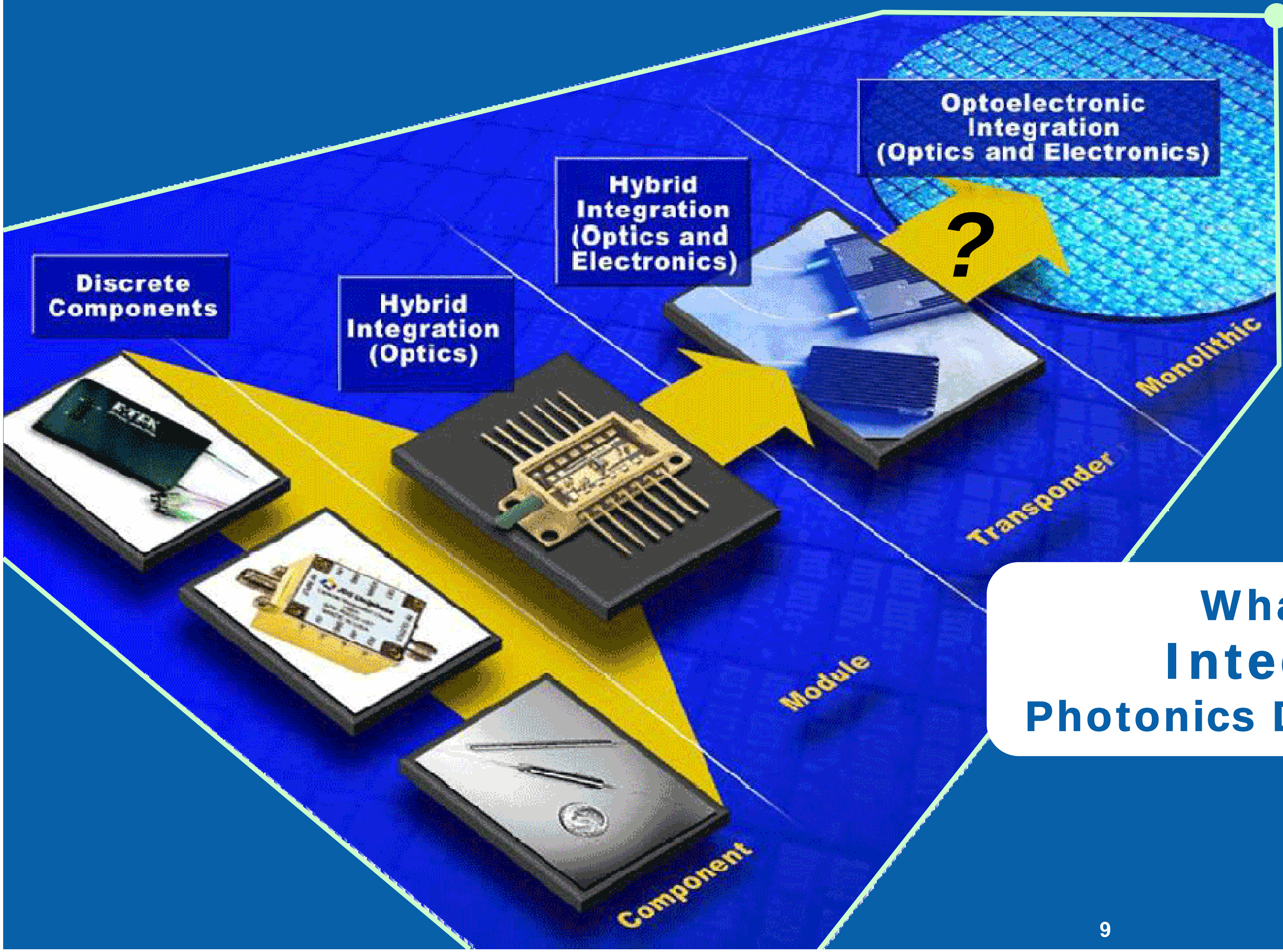


Moving to Interconnects



Drive optical to high volumes and low costs

Photonics Evolution



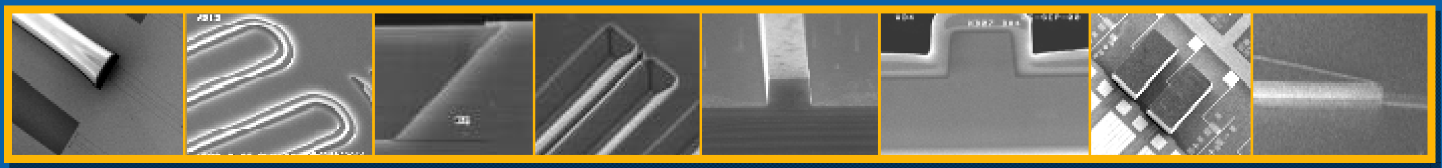
What could Integrated Photonics Deliver?

Silicon Photonics

- Motivation & applications
- History & progress
- Intel's Research Program
- Future work
- Summary

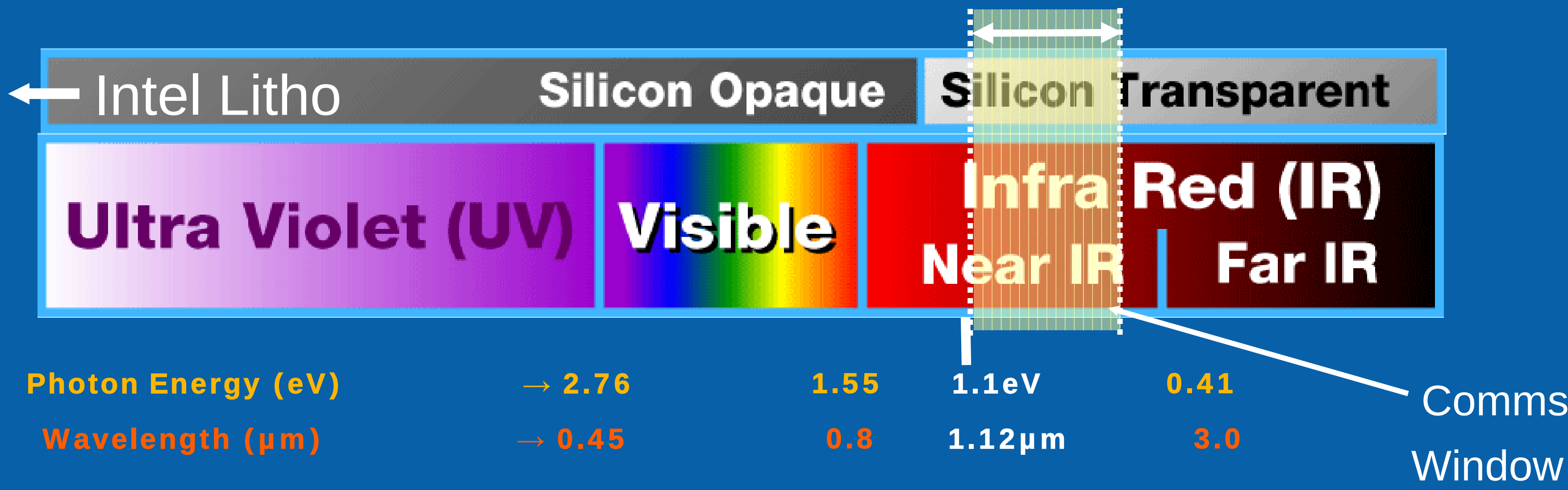
The Opportunity of Silicon Photonics

- Enormous ($ billions) CMOS infrastructure, process learning, and capacity
  - Draft continued investment in Moore's law
- Potential to integrate multiple optical devices
- Micromachining could provide smart packaging
- Potential to converge computing & communications



To benefit from this optical wafers must run alongside existing product.

Silicon as an Optical Material



- ✓Transparent > ~1.1 µm
- ✓High index
- ✓CMOS Compatible
- ✓Low cost material

- ☹ Low light emission efficiency
- ☹ No electro-optical effect
- ☹ No detection in 1.3-1.6 µm

Silicon traditionally NOT optical material of choice

Si Photonics Recent Progress

*This is not exhaustive

Pioneering work by Dr. Richard Soref (early 1980's)

2002
- Integrated APD+TIA — UT
- Inverted Taper — NTT, Cornel

2003
- Raman λ Conv. — UCLA
- Modeled GHz PIN Modulator — Surrey, Naples
- DGADC — Surrey
- PBG WG <25dB/cm — IBM

2004
- Polarization Indep. Rings — Surrey
- Raman Laser — UCLA
- >GHz MOS Modulator — Intel
- 30GHz Si-Ge Photodetector — IBM
- PBG WG <7dB/cm — IBM, FESTA, NTT

2005
- QCSE in Si — Stanford
- Stim-Emission — Brown
- CW Raman Laser — Intel
- 10Gb/s Modulator — Intel, Luxtera
- 1.5Gb/s Ring Mod. — Cornell
- 39GHz Si-Ge Photodetector — Univ. Stuttgart
- PBG WG <3db/cm — NTT

2006
- Hybrid Silicon Laser — Intel - UCSB
- Broadband Amplification — Cornell
- E-O Effect Strained-Si — DTU
- 10Gb/s SiGe PIN Commercial Quality — Intel

2007
- 40Gb/s Raman Amp & λ Conv.
- Ring Laser — Intel
- 40Gb/s Modulator — Intel
- 40Gb/s SiGe Wave Guide PIN — Intel

Device performance making significant advances

intel Leap ahead

Silicon Photonics

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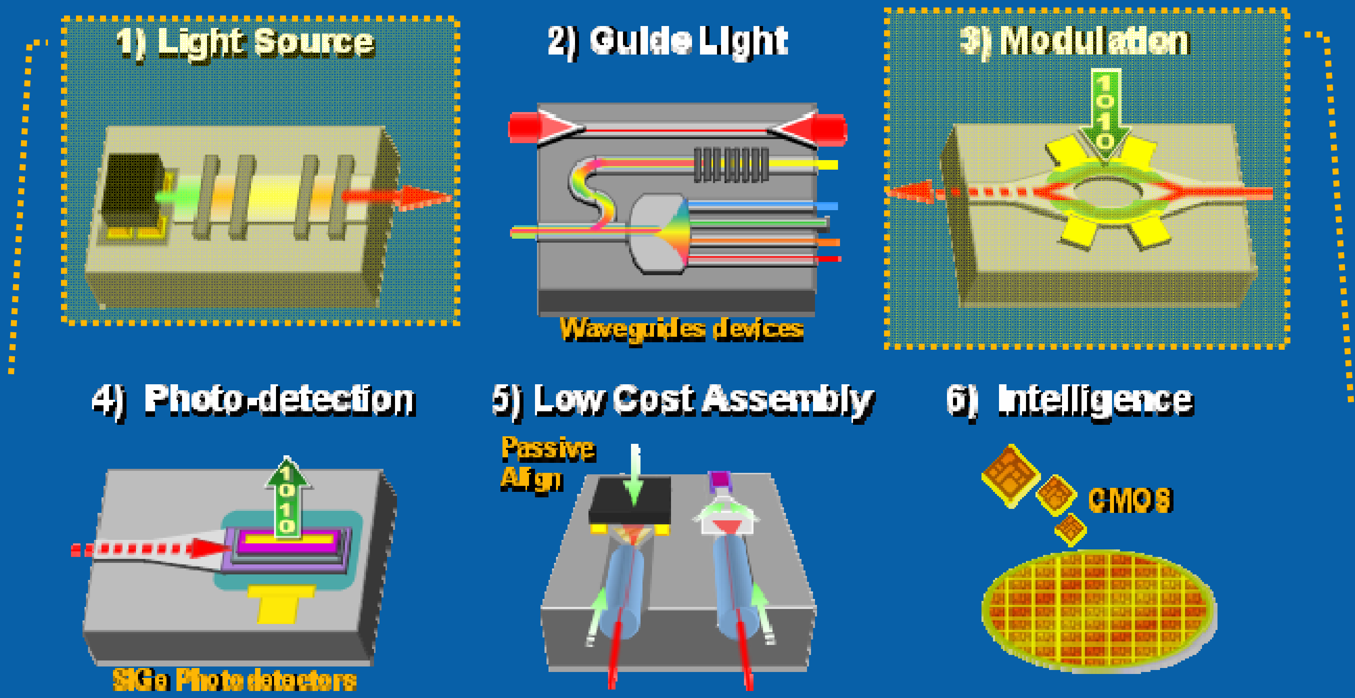
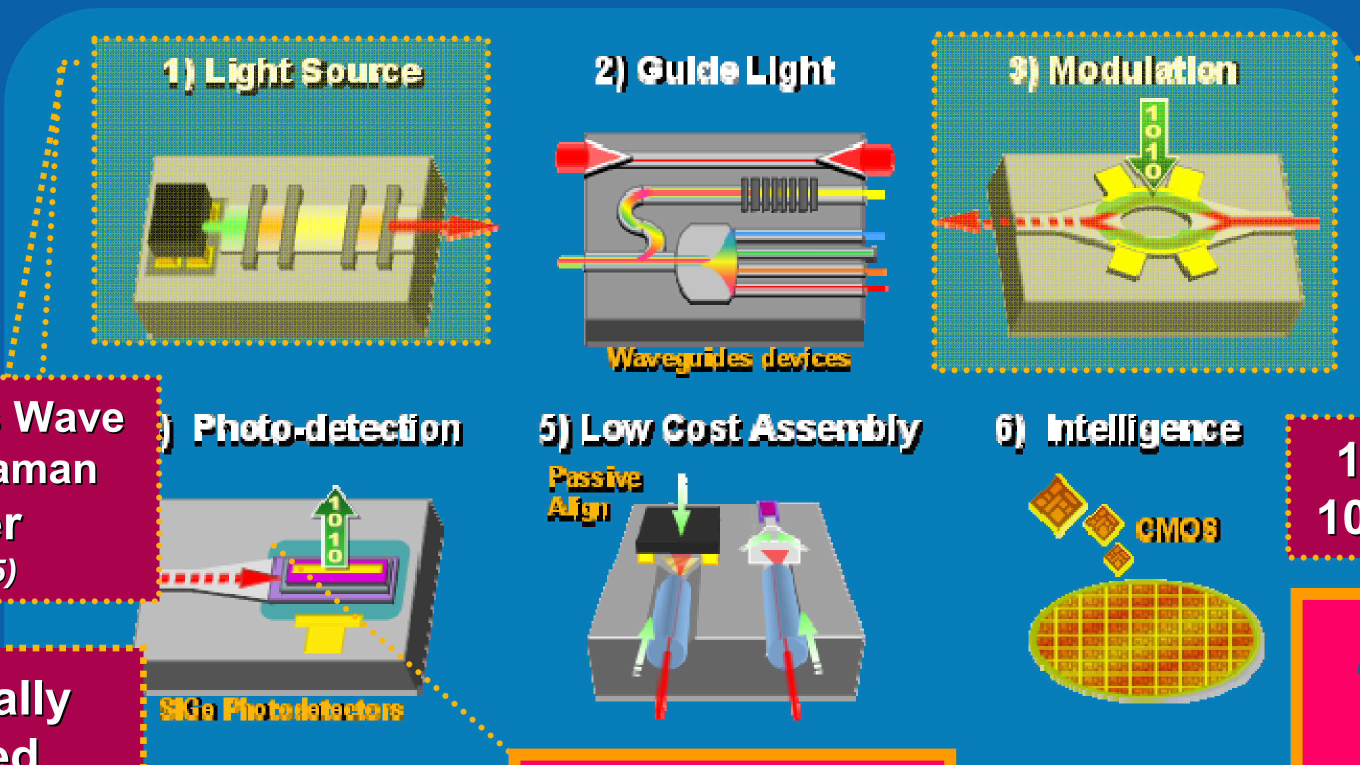
Intel's Silicon Photonics Research



First: Innovate to prove silicon is a viable optical material

Intel's Silicon Photonics Research



Continuous Wave Silicon Raman Laser
(Feb '05)

Electrically Pumped Hybrid Silicon laser
(September 2006)

40 Gb/s TODAY

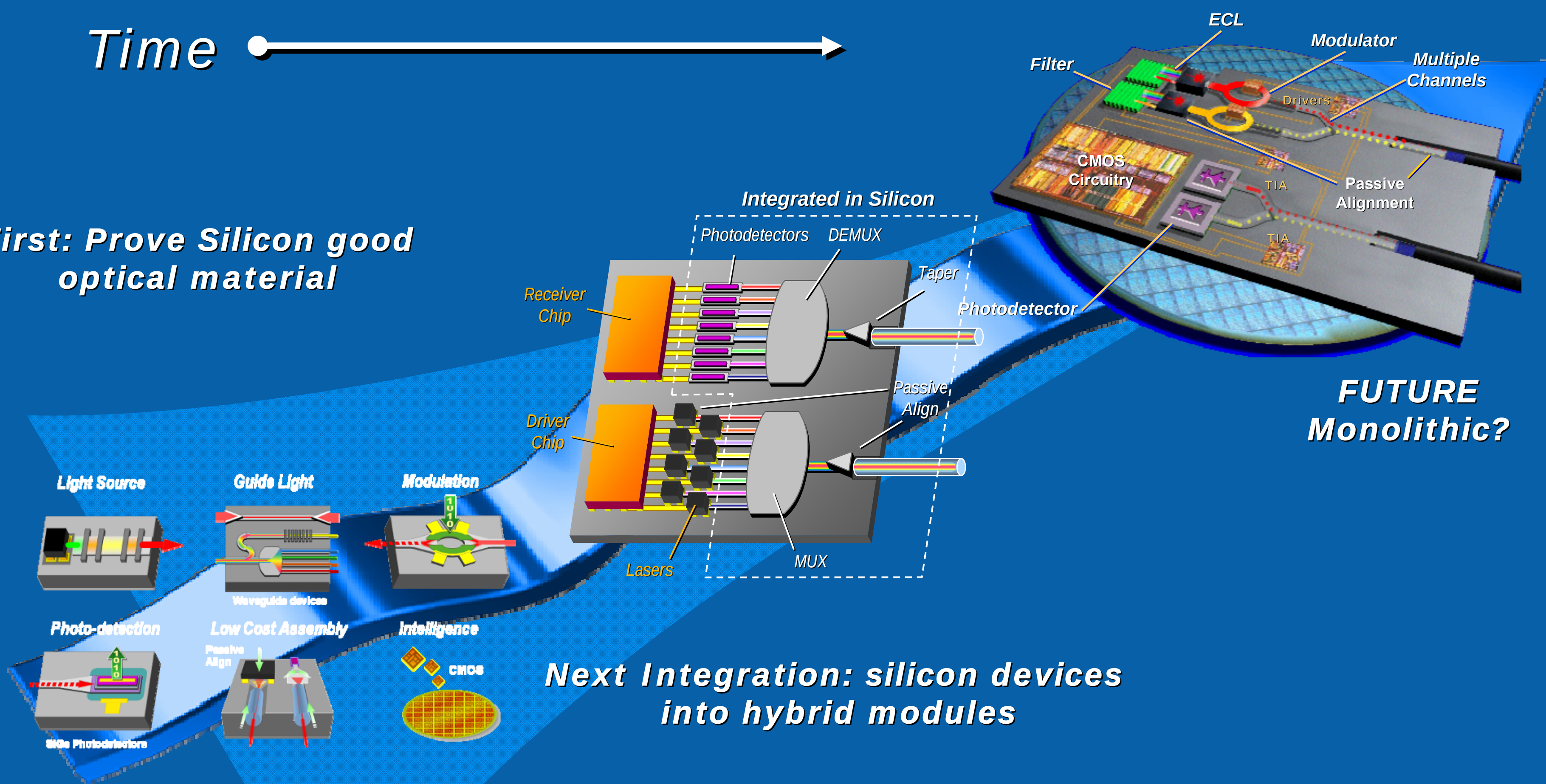
1GHz *(Feb '04)*
10 Gb/s *(Apr '05)*

40 Gb/s
(Jul '07)

Achieved 40 Gb/s for most devices
Next: Focus on integration

Integration Vision

Time



First: Prove Silicon good optical material

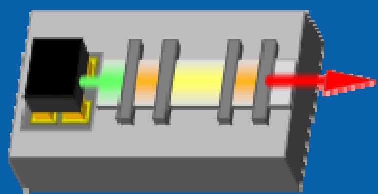
Next Integration: silicon devices into hybrid modules

FUTURE Monolithic?

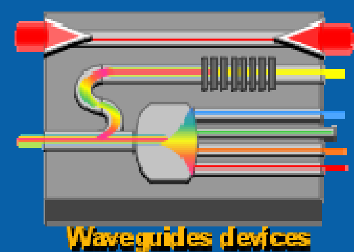
Increasing silicon integration over time

Building Block Research

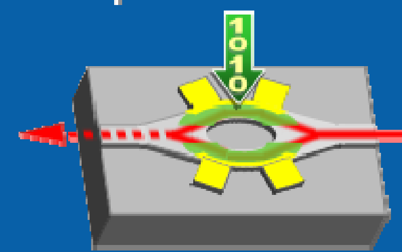
1) Light Source



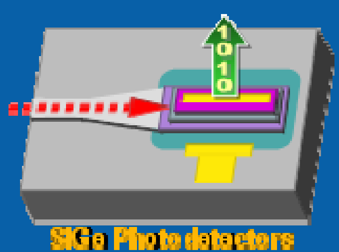
2) Guide Light



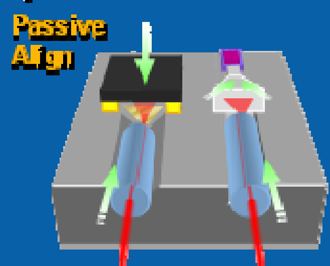
3) Modulation



4) Photo-detection



5) Low Cost Assembly

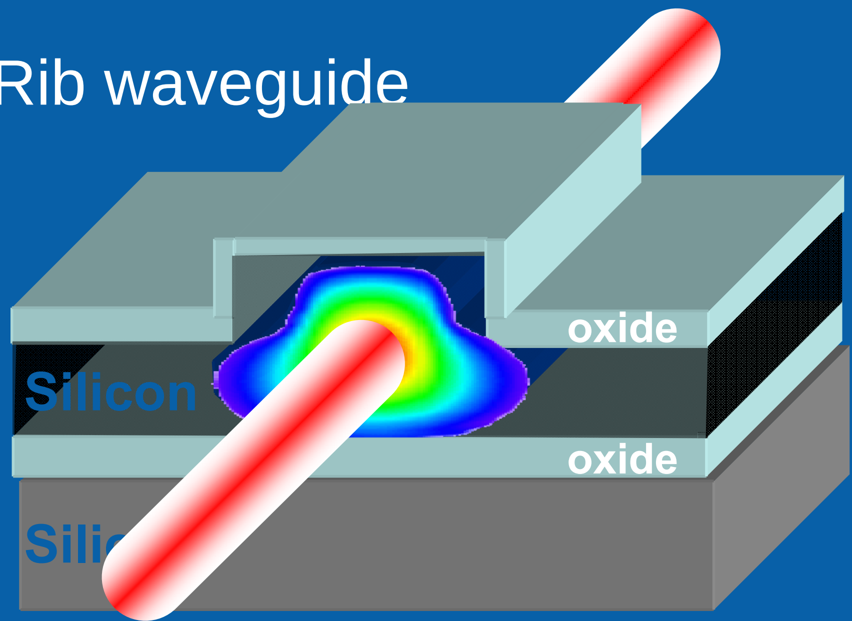


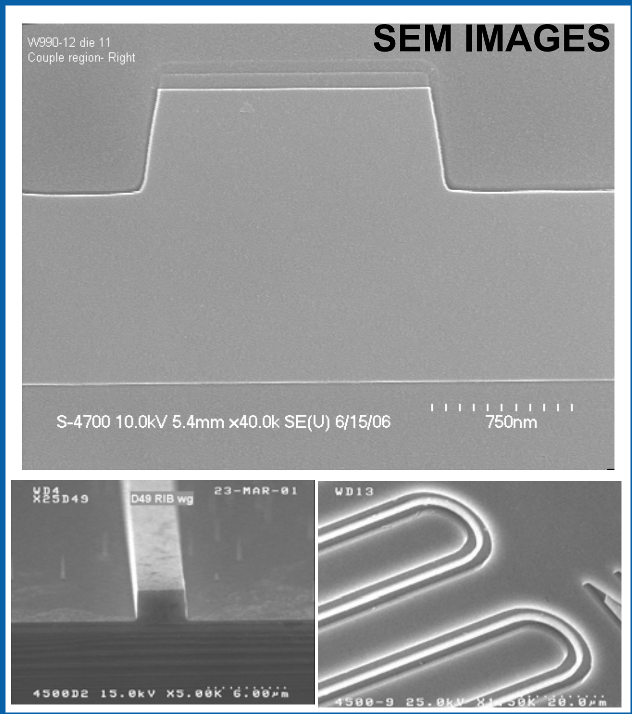
6) Intelligence

Leap ahead™

Guiding Light with Si Waveguides

Ex: Rib waveguide

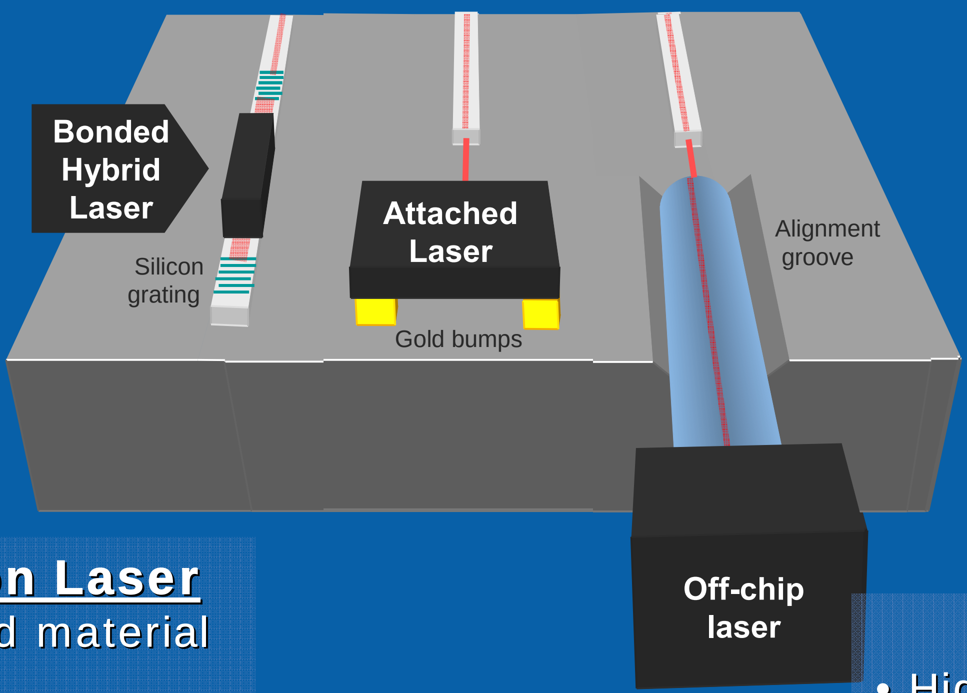




- Proven area for silicon
- High index = small structures
  - Strip and Photonic crystals for further scaling
- Splitters, couplers, gratings, AWGs, MMIs have all been demonstrated

Continue *to reduce size while maintaining performance*

Options for Integrating Light Sources



Hybrid Silicon Laser

- Bond InP based material to Silicon
- No alignment
- Many lasers with one bonding step
- Amenable to high integration
- Potentially lowest cost

Direct Attached Laser

- Tight alignment tolerances
- Requires gold metal bonding
- Passive alignment challenges
- Less Expensive

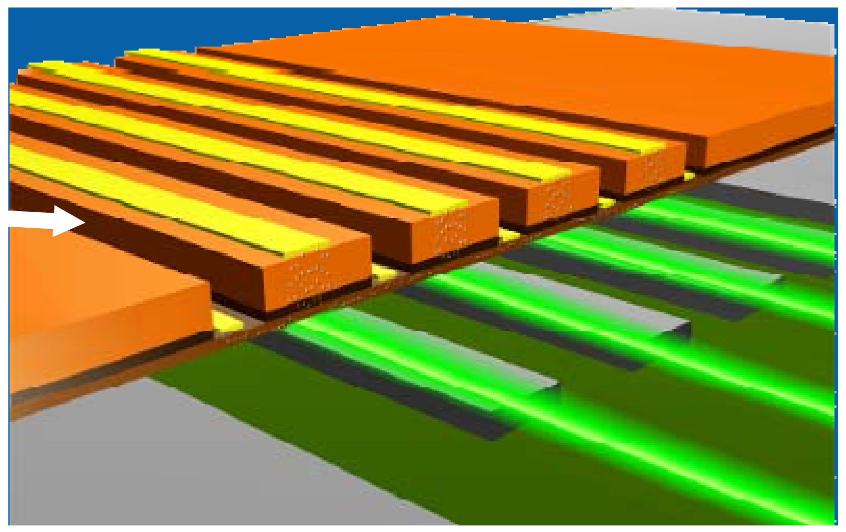
Off-chip Laser

- High power laser required
- Requires fiber attach
- Non-integrated solution
- Expensive

Hybrid Silicon Laser

Collaboration with UCSB

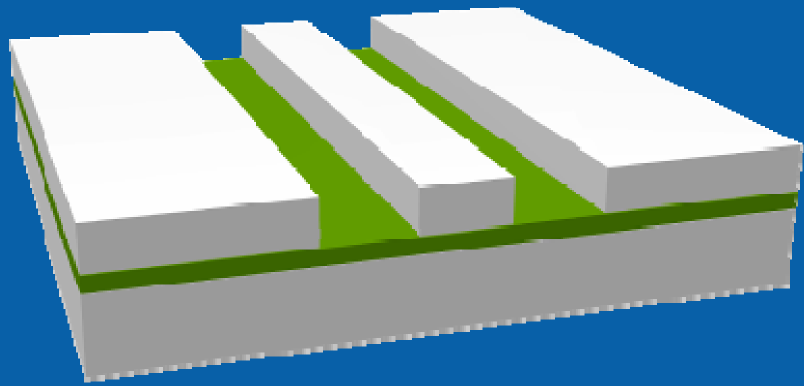
- The Indium Phosphide emits the light into the silicon waveguide



- The silicon acts as laser cavity:
  - Silicon waveguide routes the light
  - End Facets or gratings are reflectors/mirrors
  - Light bounces back and forth and gets amplified by InP based material
  - Laser performance determined by Silicon waveguide

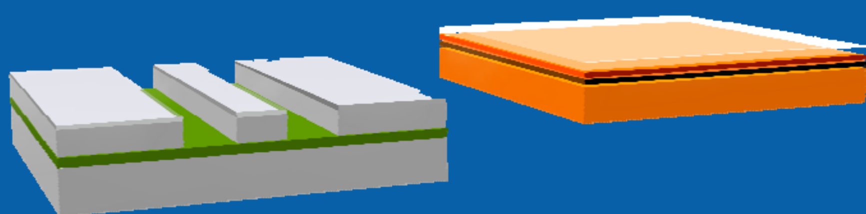
No alignment needed
10's if not 100's of lasers with ONE bond

Hybrid Laser Process

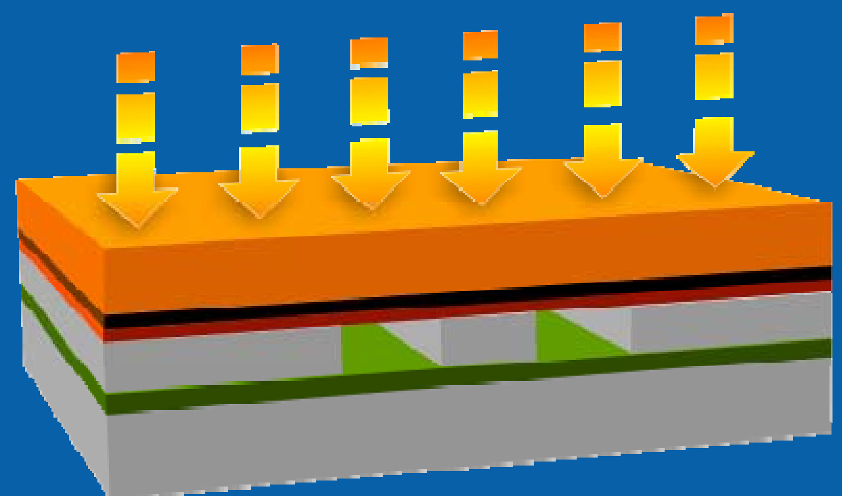


1) A waveguide is etched in silicon

2) The Indium phosphide is processed to make it a good light emitter

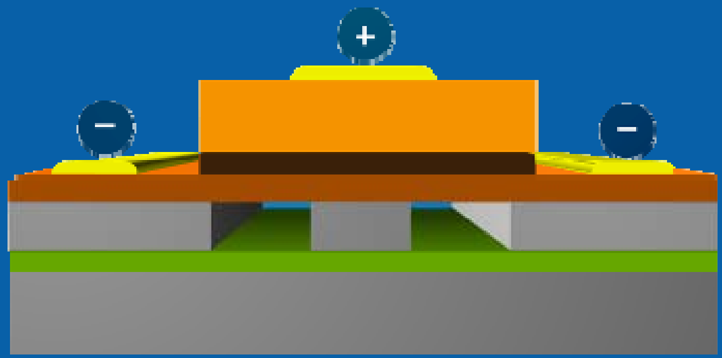


3) Both materials are exposed to the oxygen plasma to form the “glass-glue”

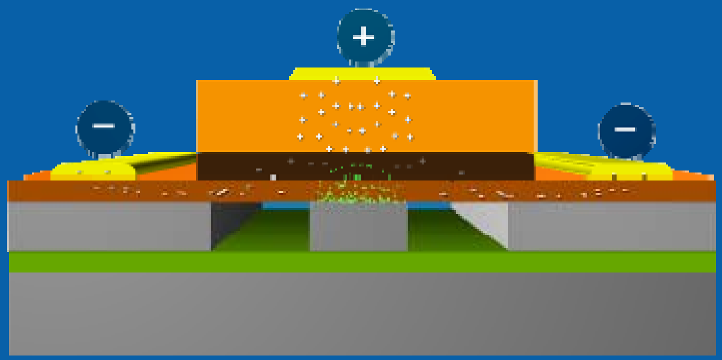


4) The two materials are bonded together under low heat

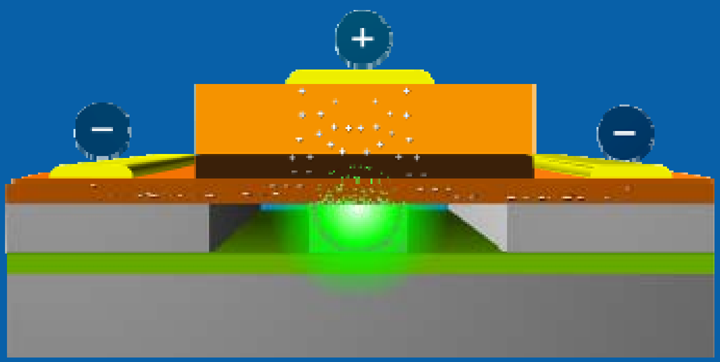
Hybrid Laser Process



5) The Indium phosphide is etched and electrical contacts are added

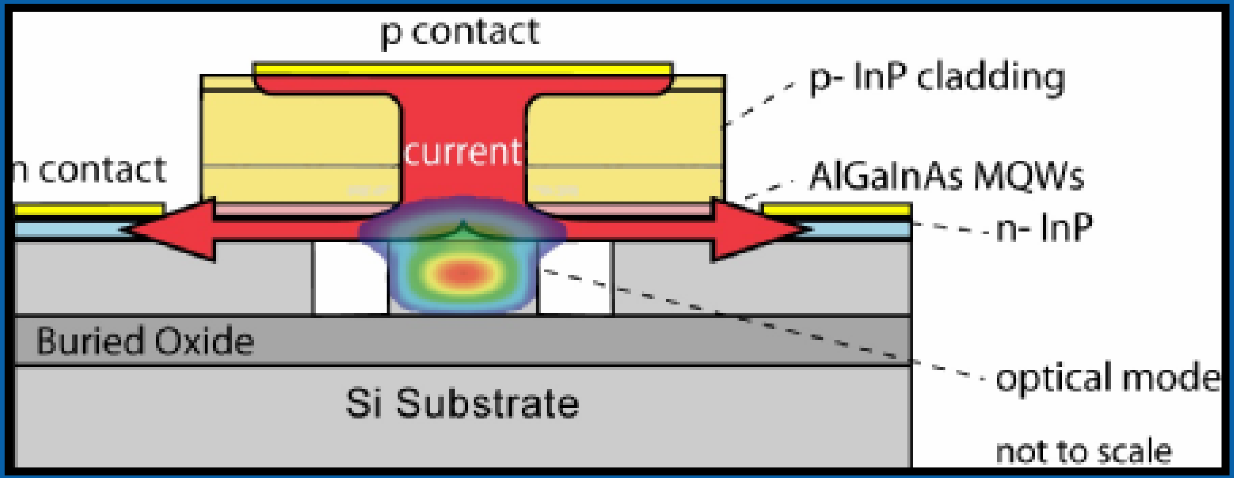


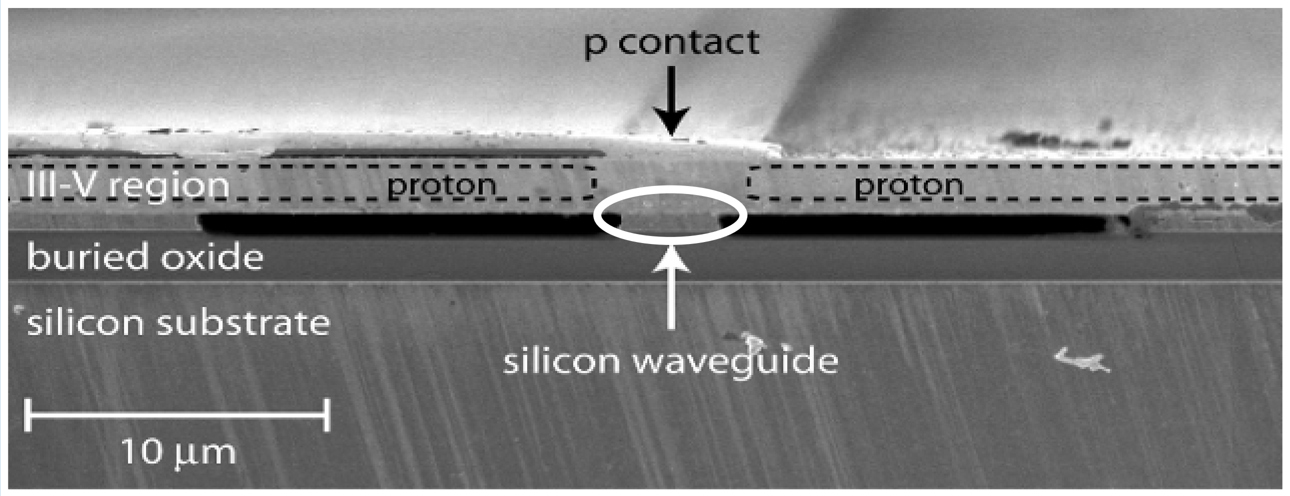
6) Photons are emitted from the Indium Phosphide when a voltage is applied



7) The light is coupled into the silicon waveguide which forms the laser cavity. Laser light emanates from the device.

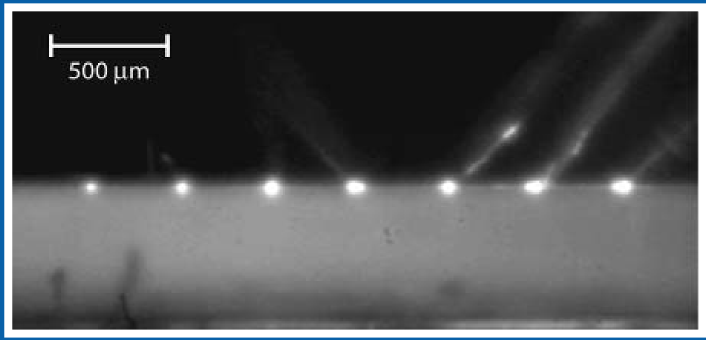
Hybrid Laser Structure



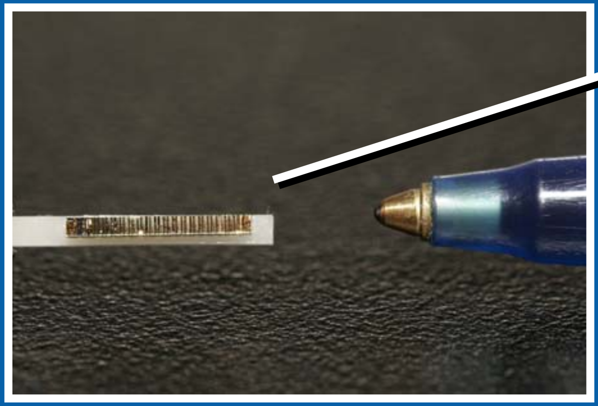


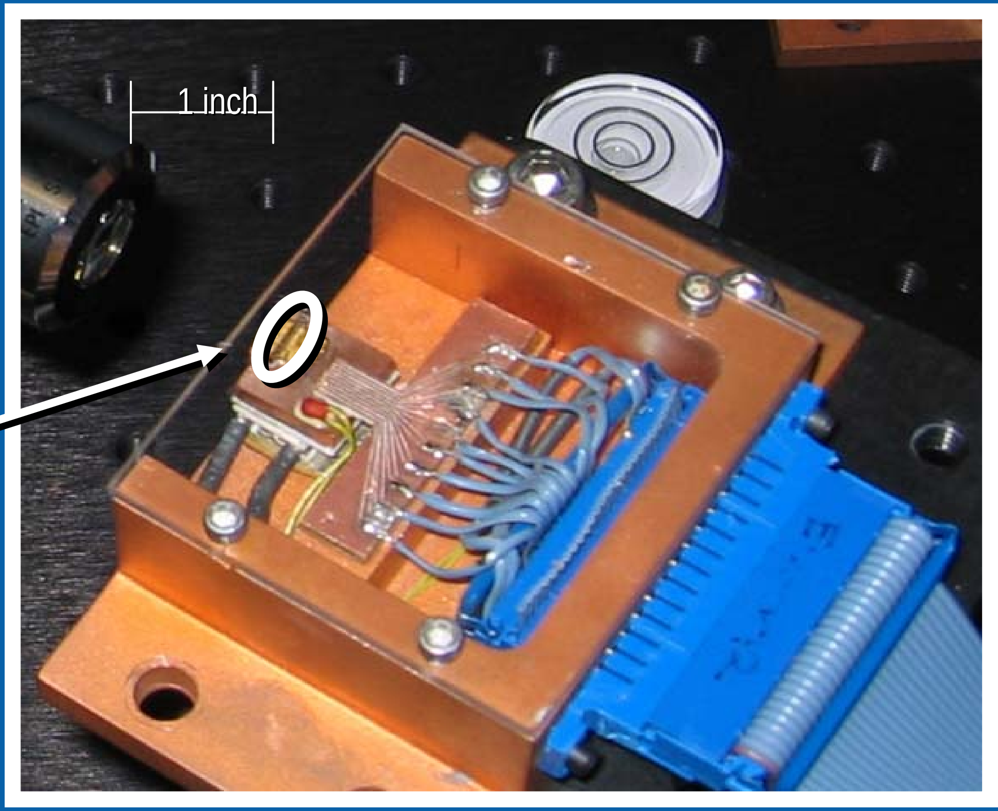
SEM (Scanning Electron Microscope) Photograph

Silicon Hybrid Laser



7 lasers outputting simultaneously

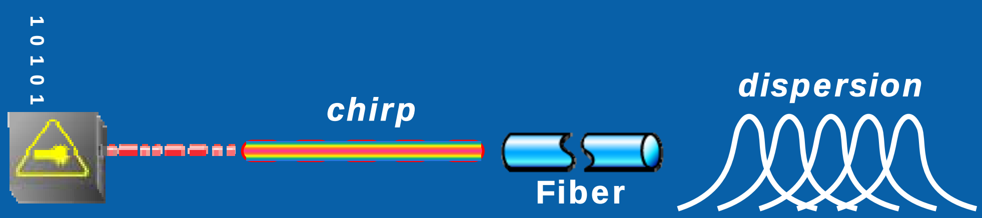




Modulation

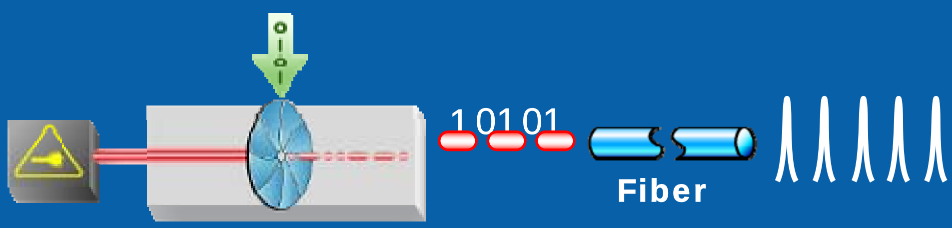
- Direct or External modulation
- External used for 10G at ~12km+

Direct Modulation



Data rate limited

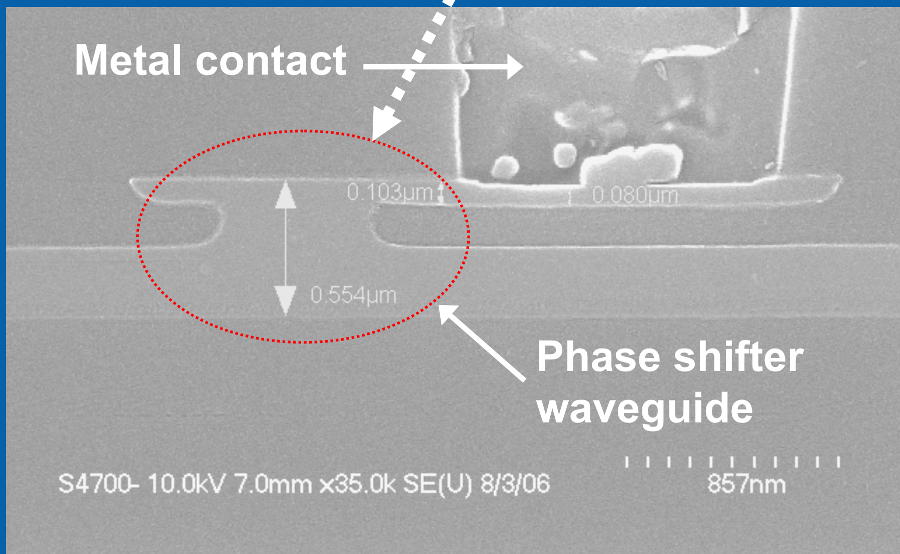
External Modulation



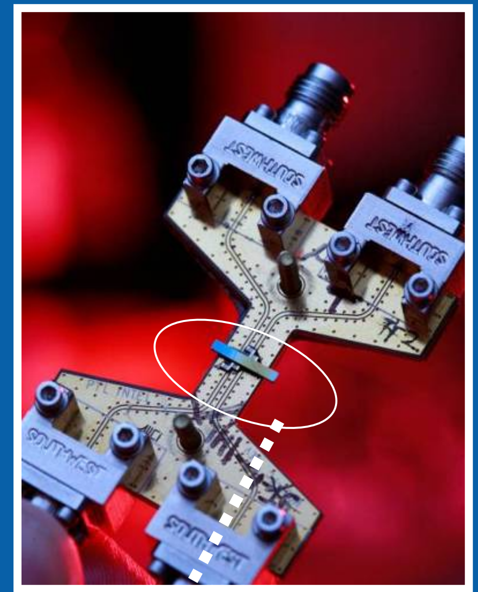
Very $$$

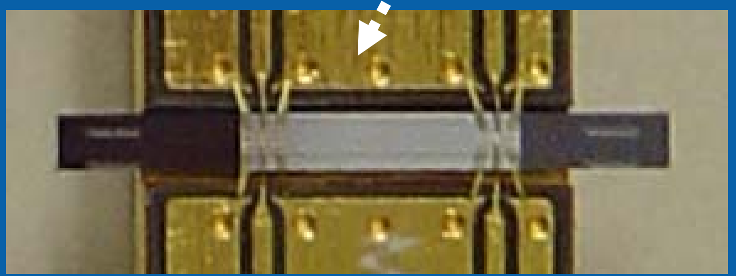
No electro-optic effect use free carriers

Intel's Second Generation: Silicon Modulator



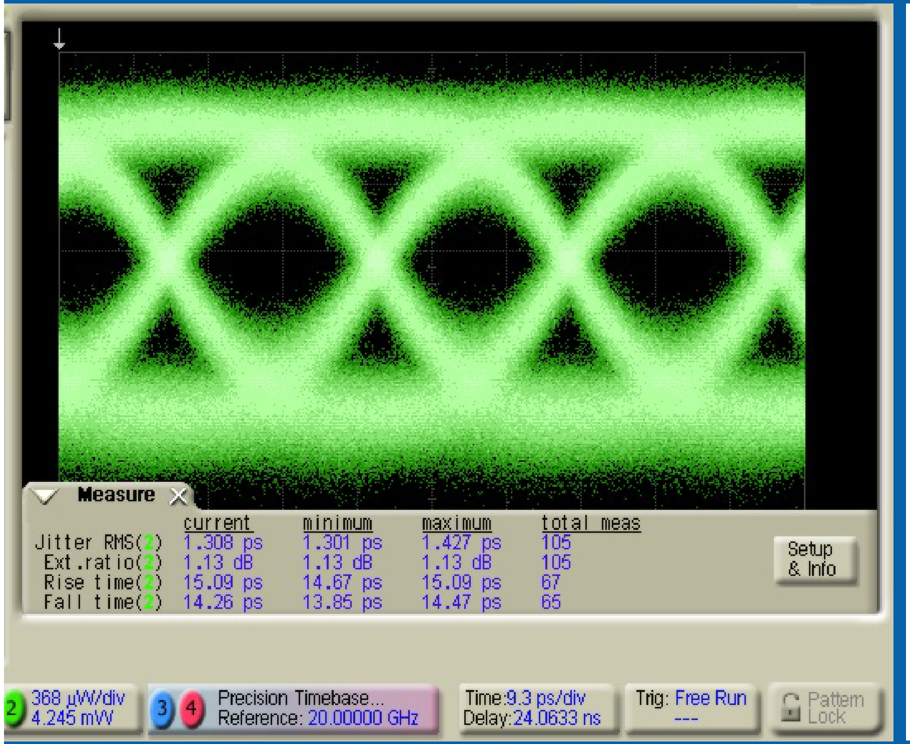
SEM picture of p-n phase shifter

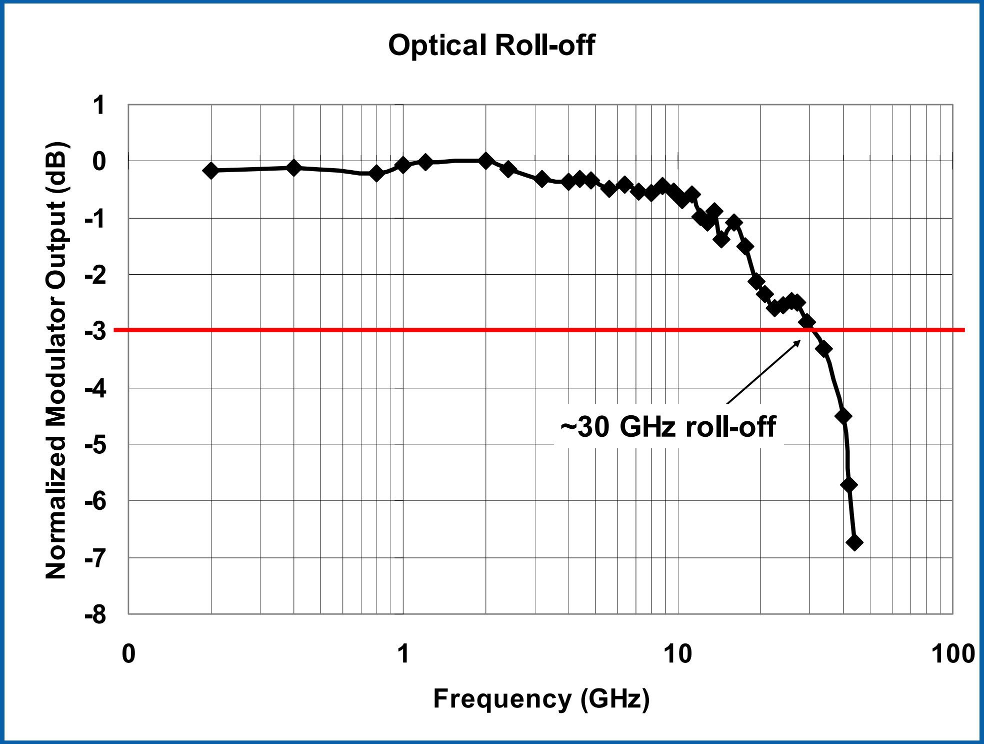




-Based on traveling wave design
-Optimized optical & electrical RF

Recent Results: 40Gb/s Data Transmission



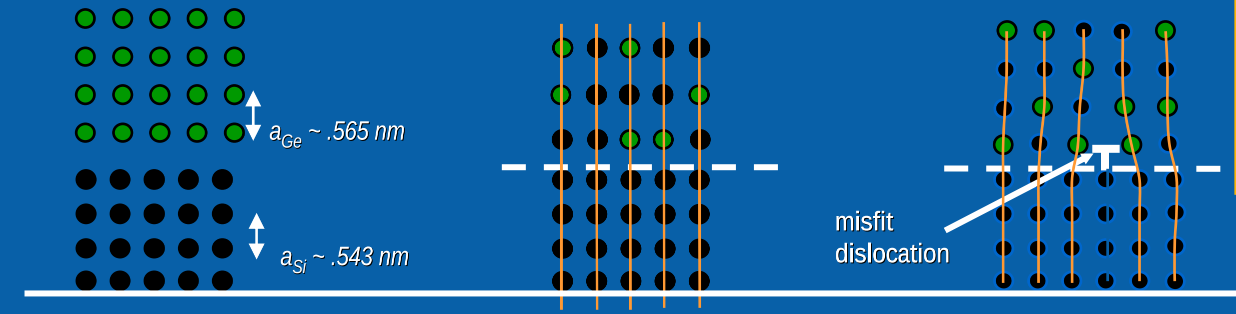


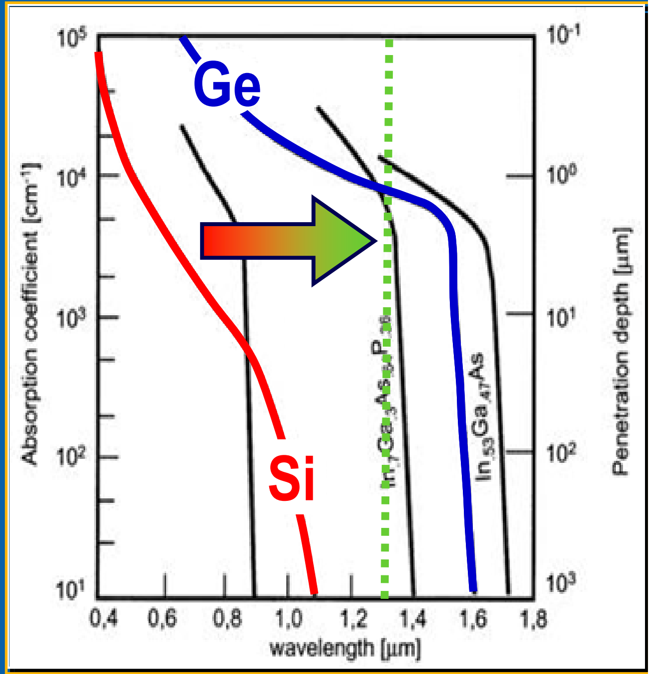
40Gb/s Data Transmission

Optical 3 dB roll off ~30 GHz

Photodetection

- Silicon does not absorb IR well
- Using SiGe to extend to 1.3µm+
- Must overcome lattice mismatch

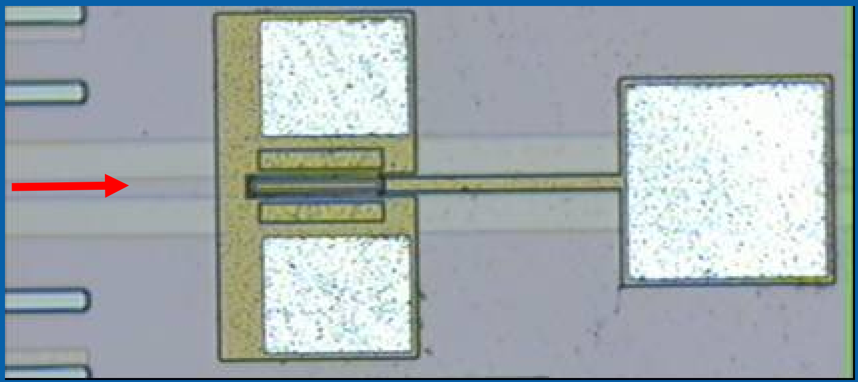




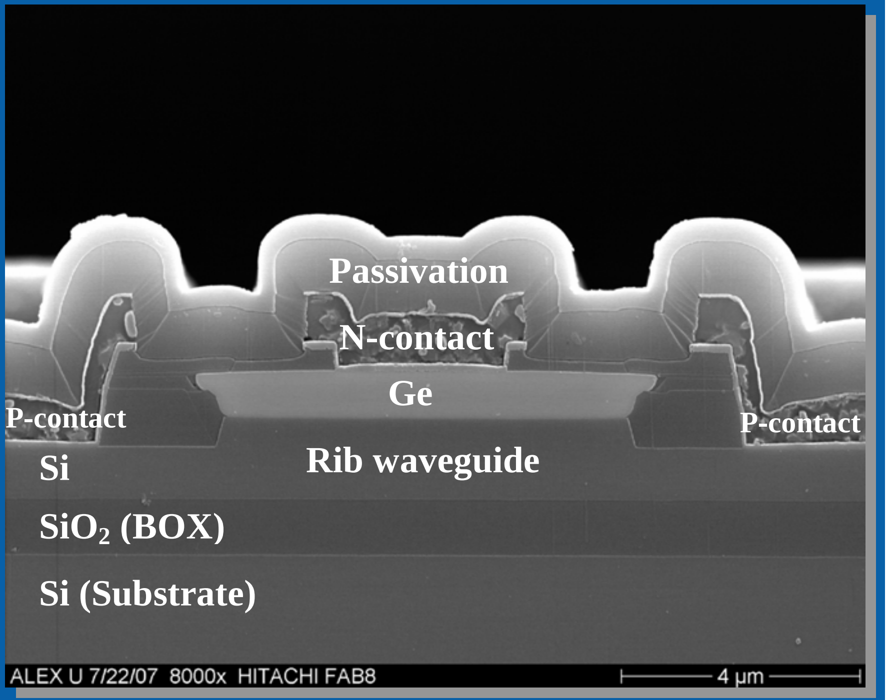
Misfit dislocations typically create threading dislocations which degrade device performance - *dark current (I_{dk}) goes up*.

Must simultaneously achieve required speed, responsivity, & dark current.

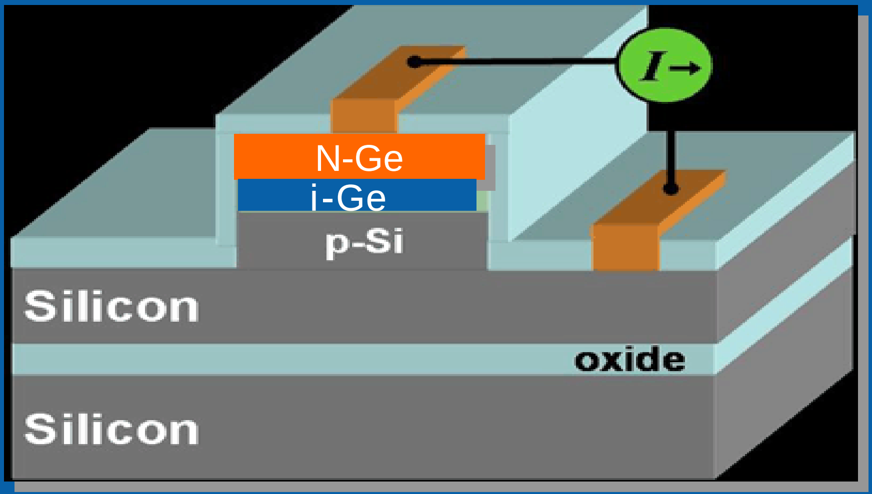
Waveguide Photodetector Design



Top View



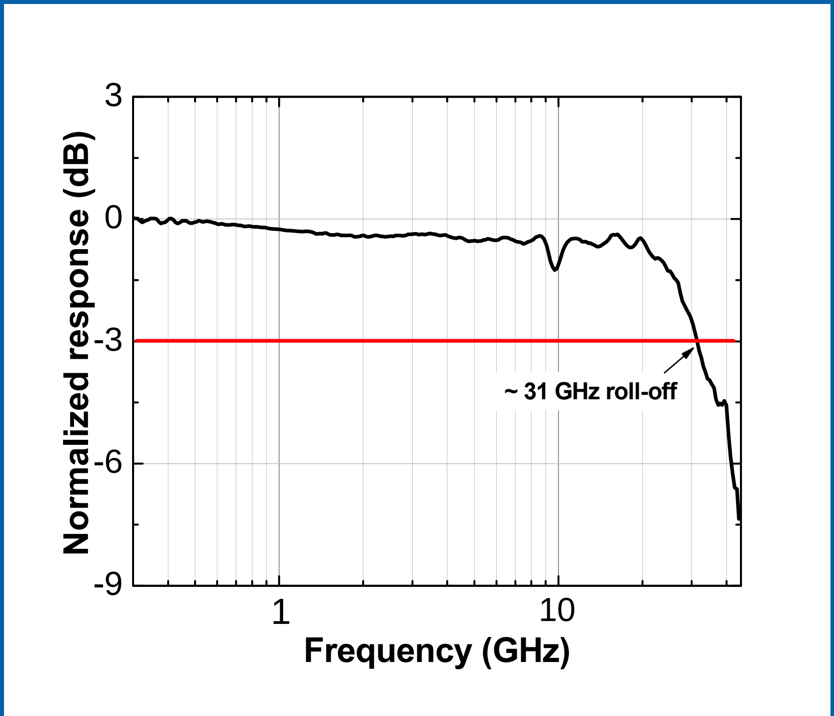
SEM Cross-Section



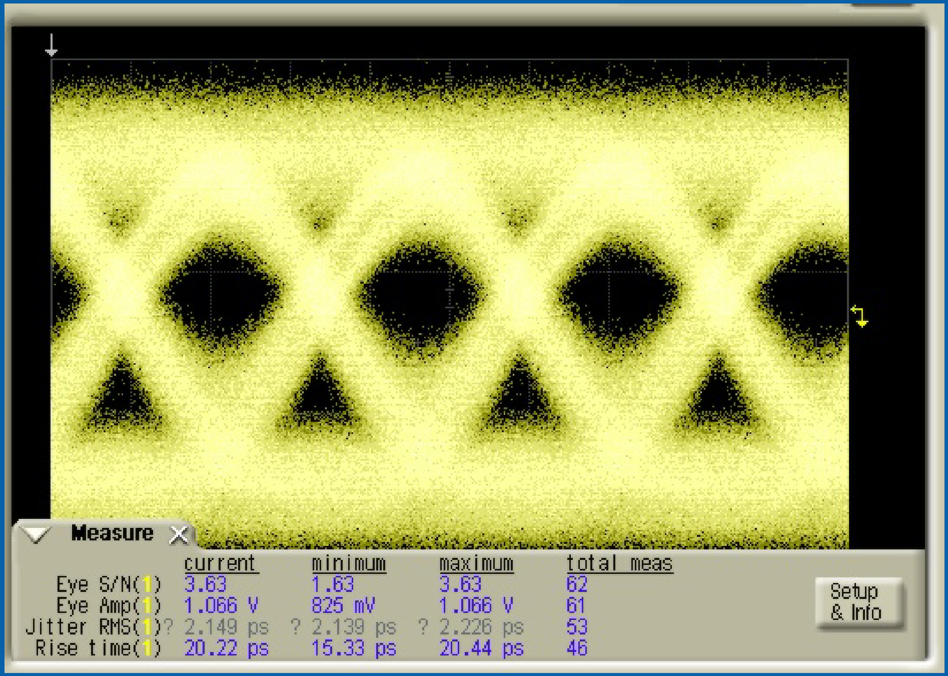
SEM Cross-Section

Experimental Results: 40Gb/s

Presented Sept 20th: Group IV conference Tokyo Japan



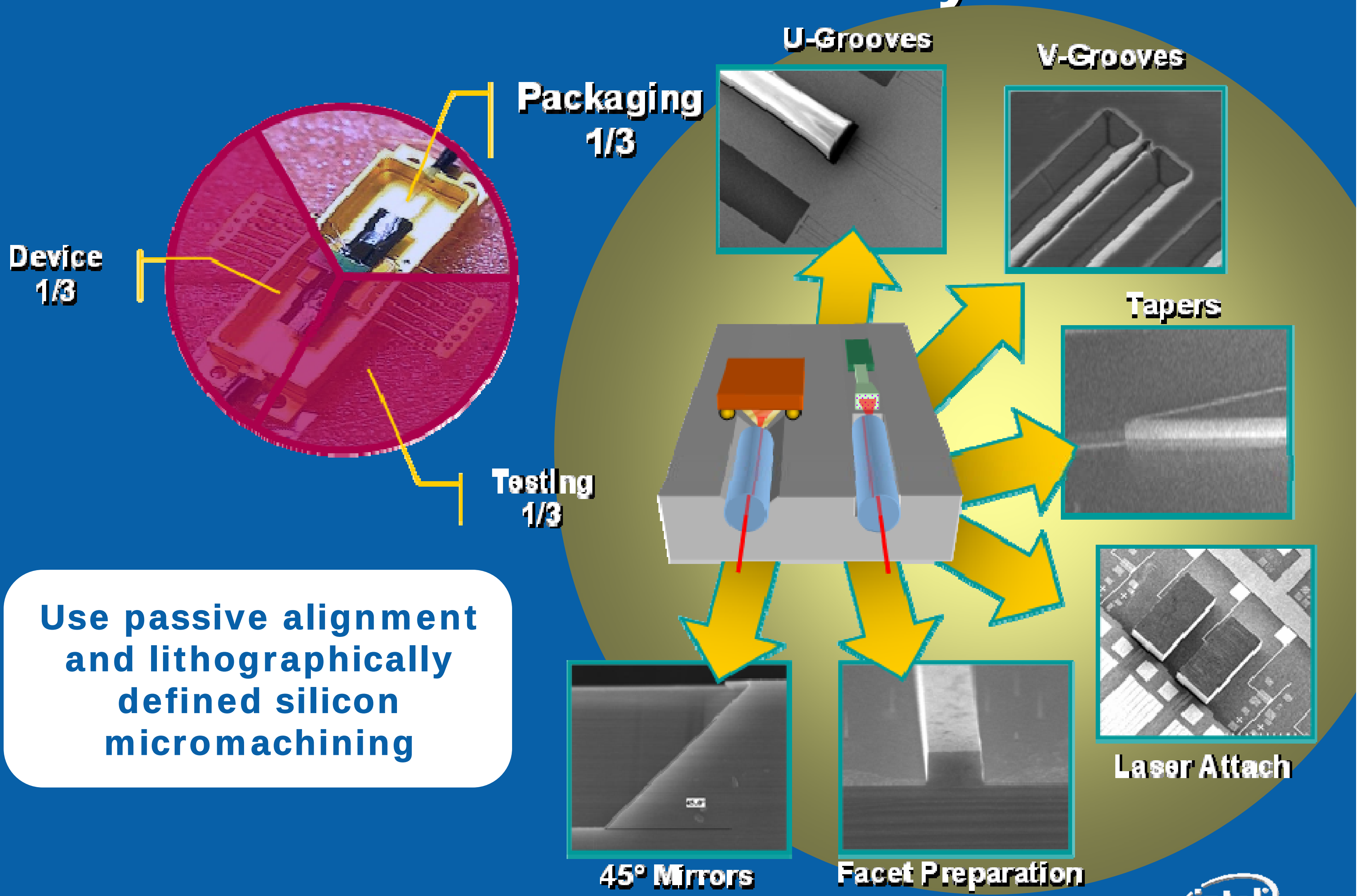
31 GHz Optical Bandwidth



40 Gb/s Data transmission

95% efficient (up to λ ~1.56um)
< 200nA of dark current

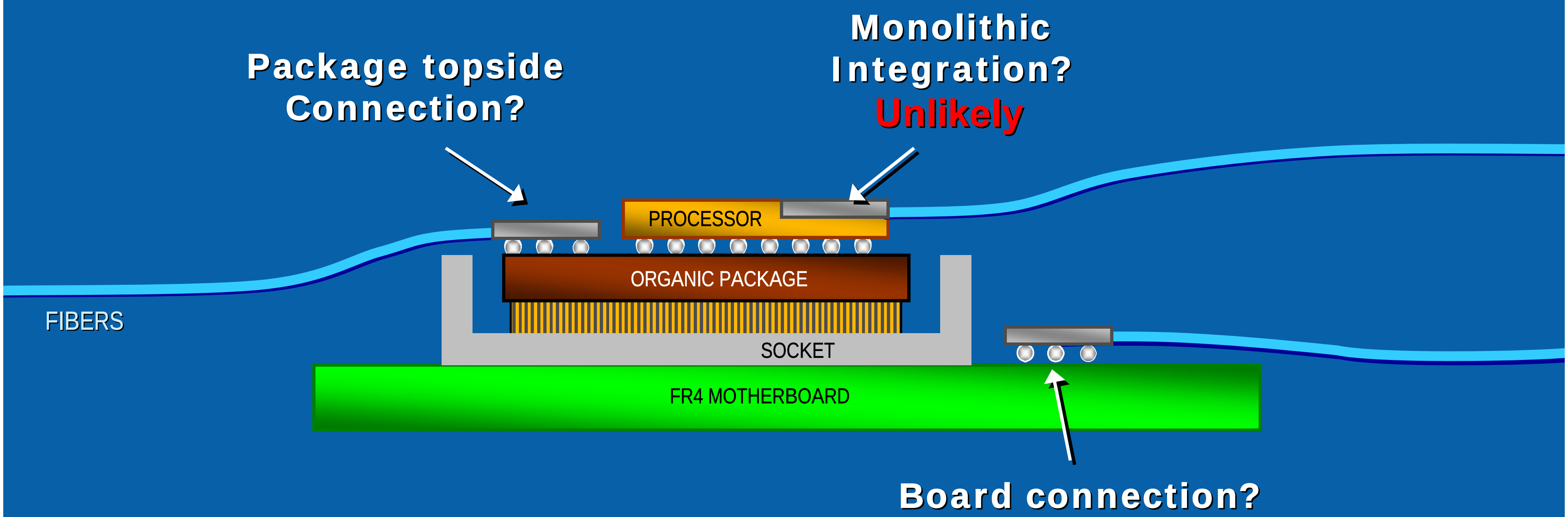
Low Cost Assembly



Use passive alignment and lithographically defined silicon micromachining

Challenge: Packaging

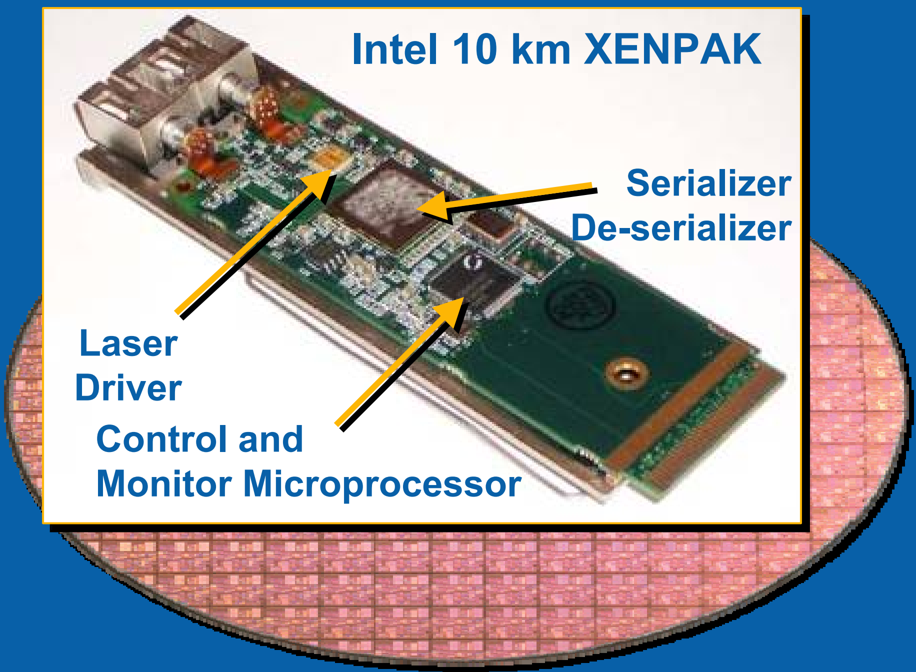
Example: Optical Interface



Issues: Connector cost, assembly cost, testing, reliability and compatibility with existing electrical packages

Multiple approaches. Must balance performance, flexibility and feasibility

CMOS Intelligence



- Electronics are needed to control photonics – no optical logic
  - Transimpedance & Limiting Amplifiers fo photodetection
  - Drivers for lasers/modulators
  - Also Clock Data Recovery, Serializers/Deserializers, etc.

Use hybrid attached CMOS electronics. Explore monolithic integration over time

Integration: Hybrid?

Photonics and electronics processed separately

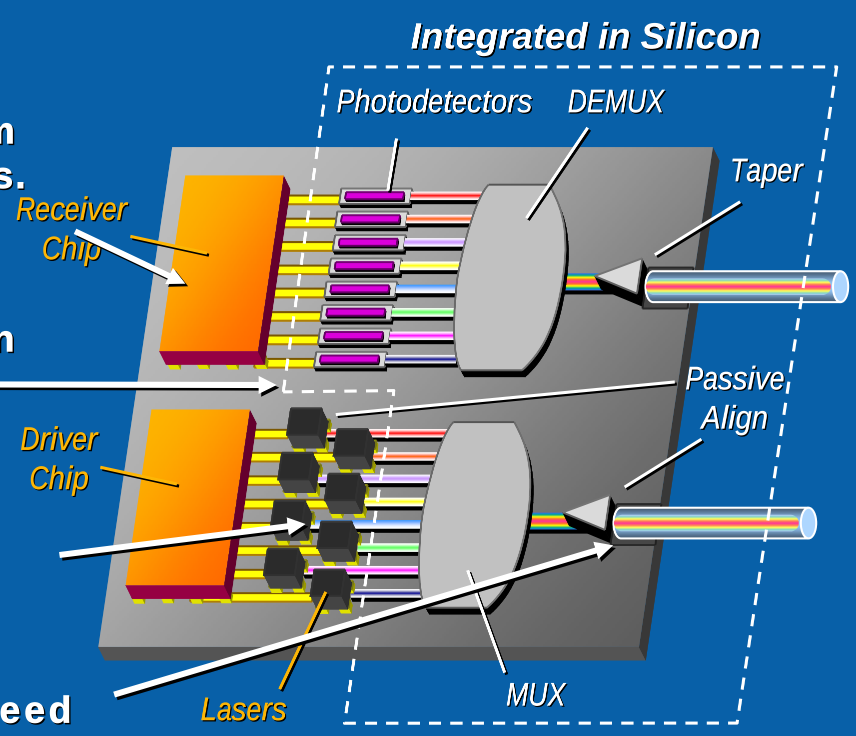
10 Gbps electronics could use < 0.13µm while optics may use older gen. process. Attachment via bumps or wirebonds.

Integration of passive and active silicon devices reduces assembly & cost.

External III-Vs: require coupling and alignment (vertical & horizontal) or direct wafer bonding to waveguides.

Both monolithic and hybrid chips will need to couple light to the outside world.

Example hybrid chip

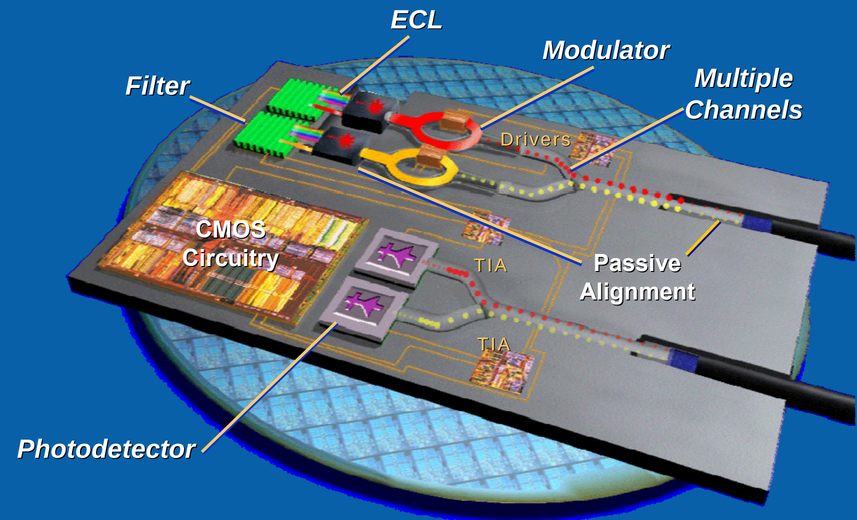


Hybrid will offer the best price-performance near term

Integration: Monolithic?

Photonics and electronics processed together on a single wafer

Example monolithic chip



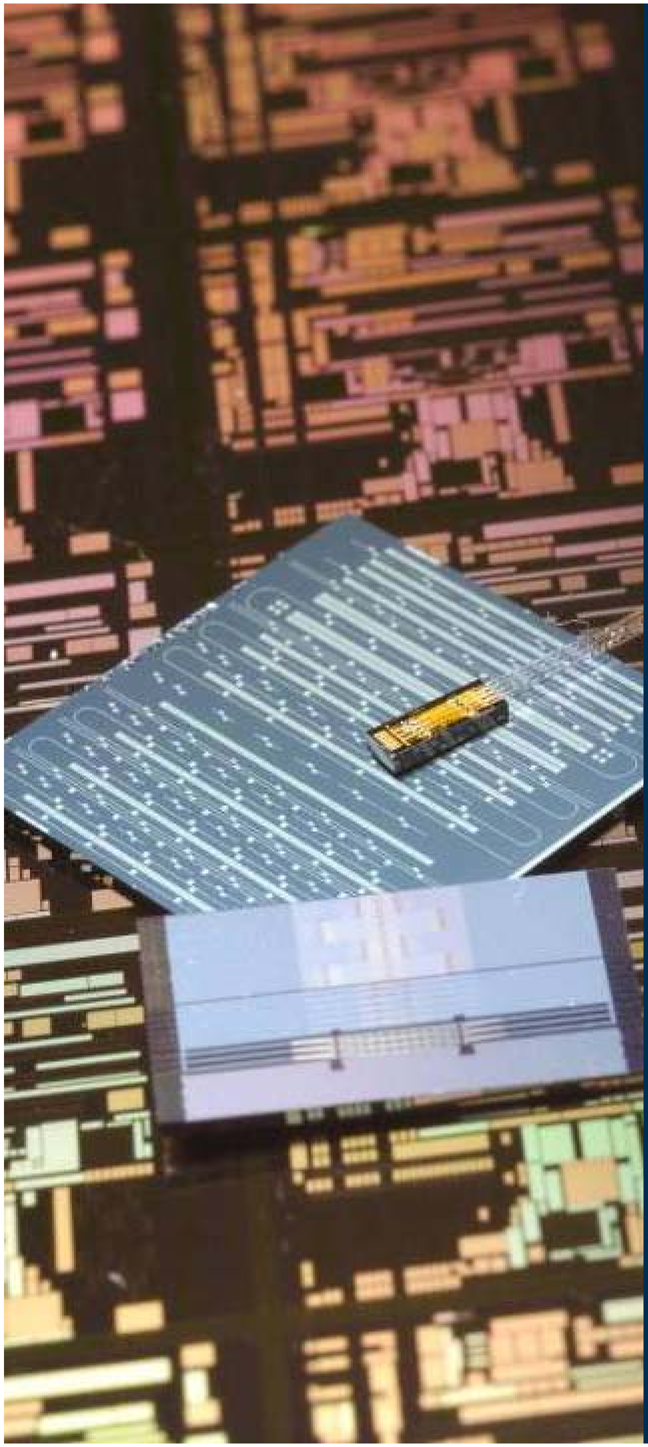
- **Motivations:**
- Performance, e.g. a Photodetector with a Trans-impedance amp
- Reduced form factor
- Cost?

- But **many challenges** for achieving high yield:

  Tighter thermal budgets, topology, metrology, complexity, etc.

Yield issues make monolithic a longer term proposition

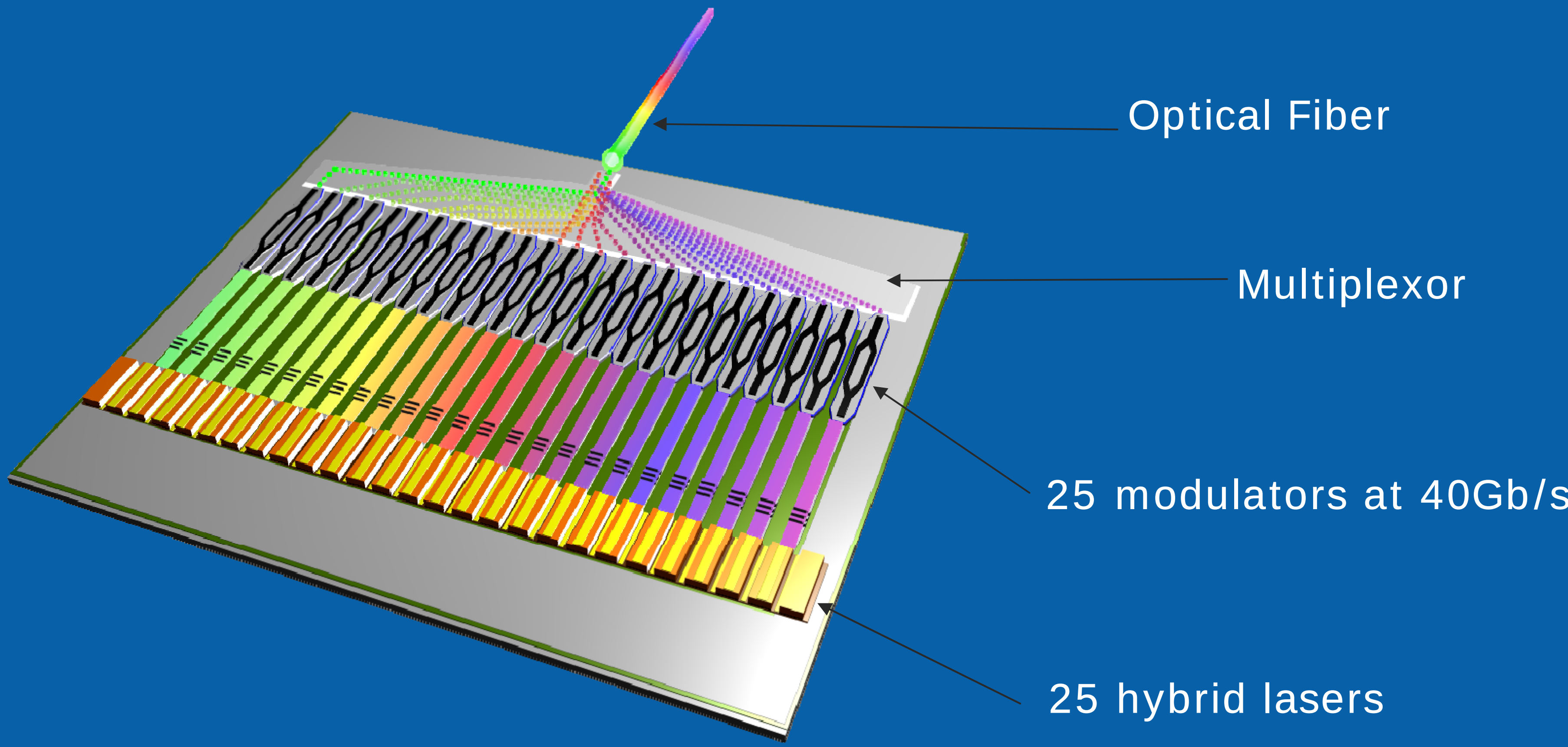
intel Leap ahead



Silicon Photonics

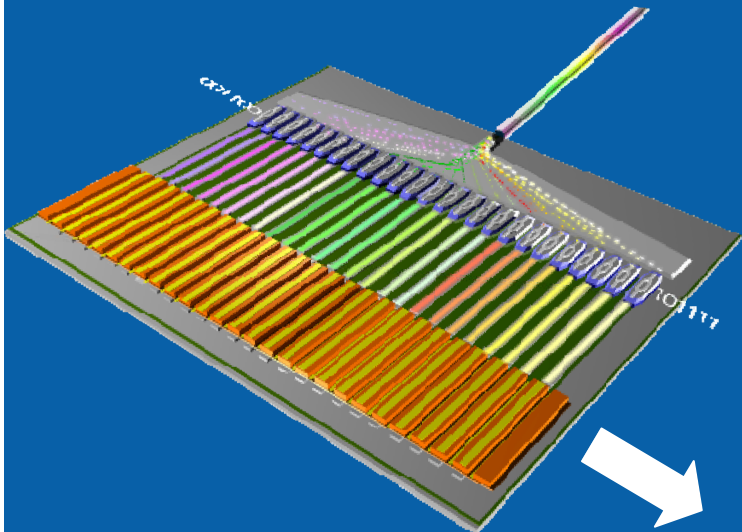
- Motivation & applications
- History & progress
- Intel's Research Program
- Future Work
- Summary

Where are we going?

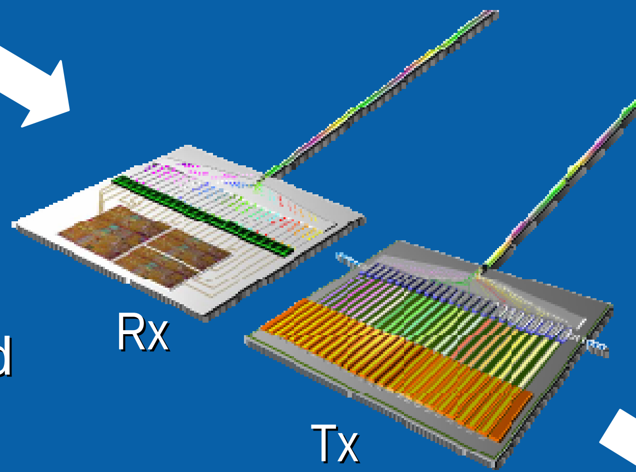


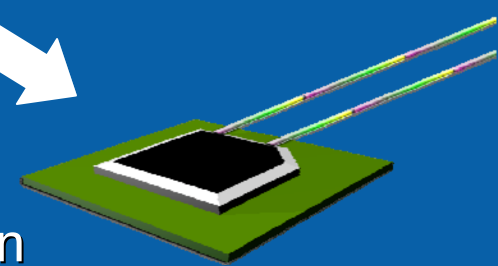
An future integrated 1 Tb/s optical link on a single chip

Integrating into a Tera-scale System



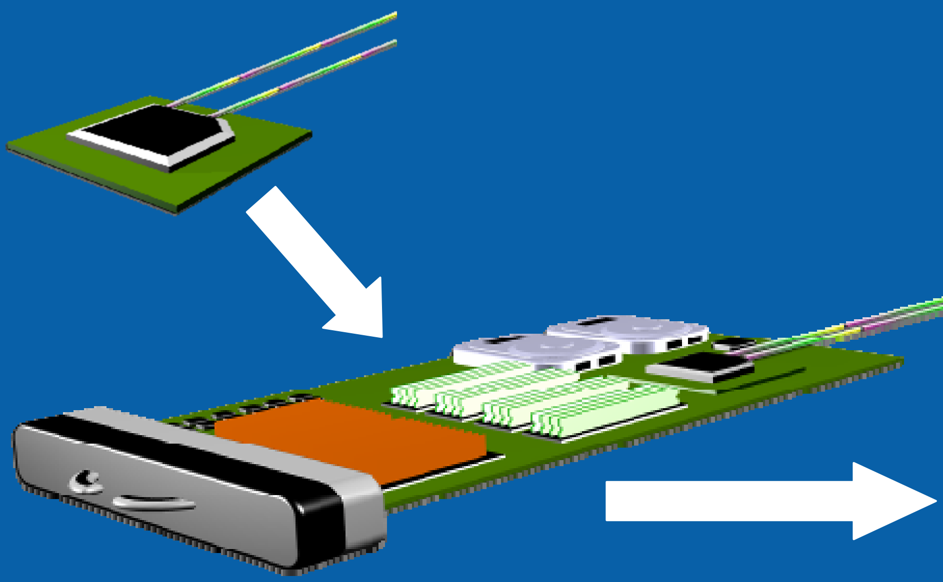
This transmitter would be combined with a receiver





Which could then be built into an integrated, silicon photonic chip!!

Integrating into a Tera-scale System



This integrated silicon photonic chip could then be integrated into computer boards

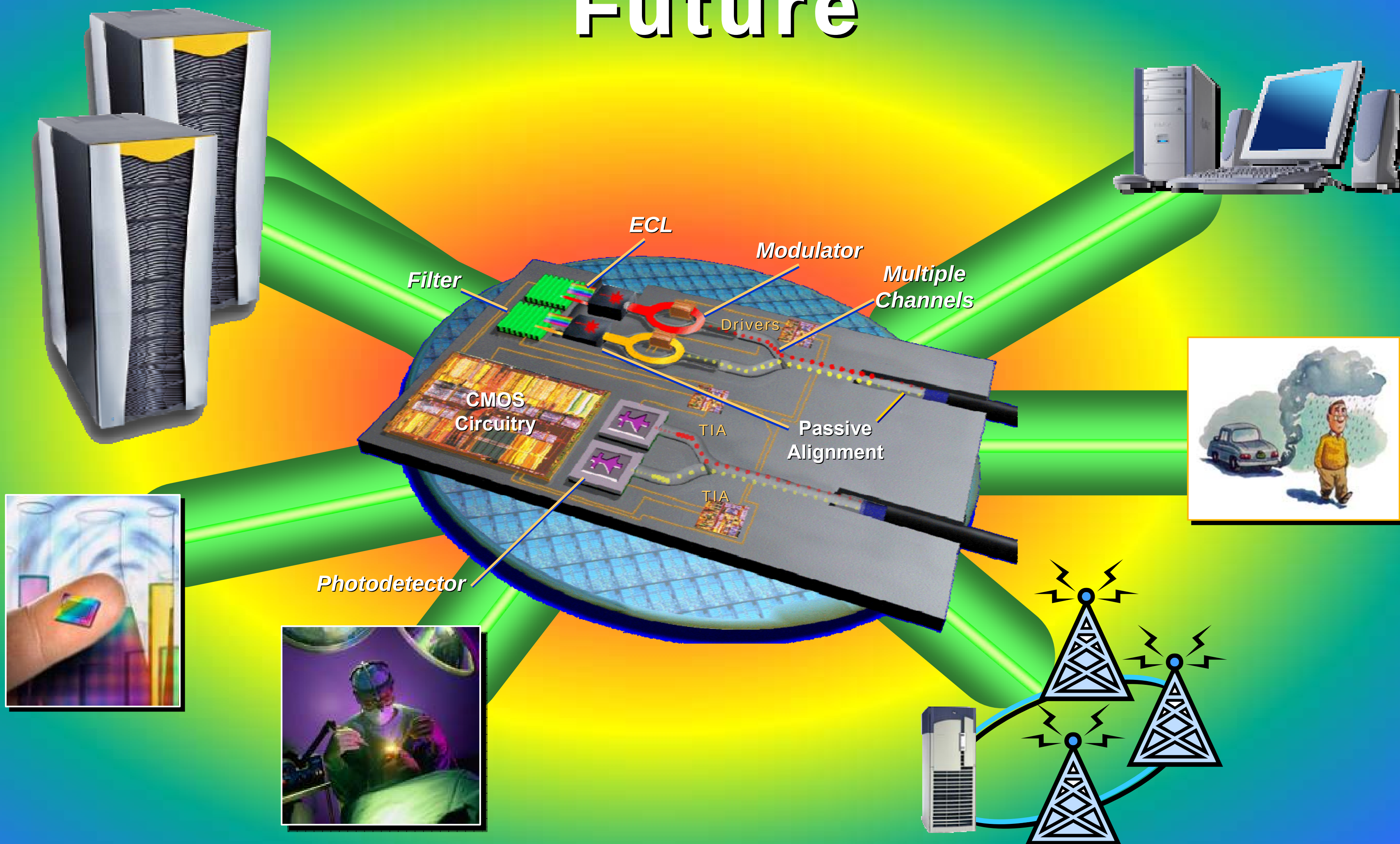
And this board could be integrated into a Tera-scale system

Summary

- Long term, convergence opportunities will be in silicon
- Silicon photonic device performance advancing at an accelerated pace.
  - Need to continue to push performance (i.e. 40G, 100G...)
- Next phase of challenges will be with integration.
- For interconnects, need to optimize electronics & photonics
  - Packaging, power, signaling, and cost will be key

If successful volume economics could allow silicon photonics to impact many areas from communications to bio to medicine

Silicon Photonics' Future



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